Realization of MOS-C Sixth Order Band Pass Filter Using FDNR

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Abstract

In this manuscript, the sixth order Band Pass Filter has been modified using FDNR. The FDNR consists of two CCII-, two capacitor and two resistor. The passive resistances are replaced by the MOS-resistor. The circuit is simulated using CMOS 0.18µm technology parameter and result obtained using PSPICE simulation software.

Keywords- *current conveyor, frequency dependent negative resistance.*

I. INTRODUCTION

There are several types of filters in analog circuits. In the radio frequency communication there is use of band pass filter that plays a pivotal role in the field of electronics communication. In the analog communication system, narrow band signals play a broad area of telecommunication application as radio television, broadcasting, mobile telephony etc. The application of narrow band signals in analog system found a wide variety of telecommunications systems including radio, television and mobile telephony. In the above applications there is use of a very narrow band signal bandwidth that is having near about 1% of the carrier frequency. If somewhere we need the application of superheterodyne receiver for intermediate frequencies in that case there is also use of narrow band signal.

It is known as the modern analog circuits are focused on the current conveyors and based on its active element having lead to lots of applications for the different analog circuit designs such as signal processing circuits, different types of filters, amplifiers, oscillator impedance convertors etc that provides different advantages such as wider bandwidth, lower power consumption, simple circuitry, greater linearity over voltage mode devices as op-amp [1]-[5].

For implementation of a circuit having nature of high quality RC-active filter, Bruton [10] has consider a number of techniques for implementing high quality RC-active filter. This technique includes use of FDNR in the analog ladder type of filter circuit. Bruton found that how the FDNR based filter circuit correlated to the RLC based circuit in respect to their passband insensitivity. From that evaluation he conclude that for the designing of the higher order (ten or higher) transfer functions there are the circuit must be with high Q's and very sharp cut-off. In the analog system the FDNR based filters can be made able to tune and implement or designed in direct from LC based filter circuits using some approximation. With the help of FDNR, design of an active filter circuit is easy from passive filter circuit. The proposed work is based on a floating CMOS designing parameters having use of FDNR topology, presents a sixth order band pass filter. Here the FDNR used, is a floating type compact and ability to suit for having a very low voltage operations and also provides higher tunability. Here a sixth order band pass filter with 40MHz cutoff frequency has been designed using the parameters of the 0.18µm CMOS process.

II. THE PROPOSED MOS-C FDNR

The negative current conveyor of Second generation (CCII-) is illustrated as below in Fig. 1. It is a three port device and it has the parameters as shown in the given matrix (1):

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \qquad (1)$$

Due to the popularity of the current conveyor of second generation, it is most widely used as a basic building block for analog circuit implementation. It can be realize as all the four controlled sources, negative impedance convertor, negative impedance inverter and so on in the analog electronics so that the number of circuits can be designed with it in simpler and easy way.

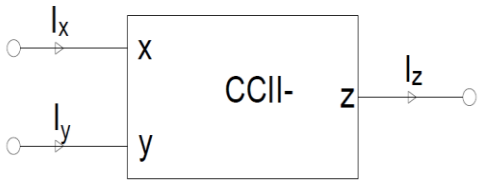

Fig. 1. Second Generation Negative Current Conveyor

The I_x is x terminal input current and I_y is the y terminal input current and I_z is the output current. The relations between these three currents are understood by the above matrix shown. Most of the literature made the second generation negative current conveyor using two second generation positive current conveyor [12] as shown below Fig. 2.

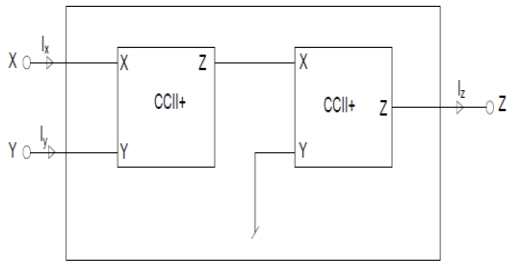

Fig. 2. CCII- Implementation using two CCII+s

The FDNR circuit of floating type is to be proposed is illustrated as below in Fig. 3. Where it requires two floating capacitors, four active MOS resistors and two negative type of current conveyor of second generation where the analysis between terminals 1 and 2 is given below.

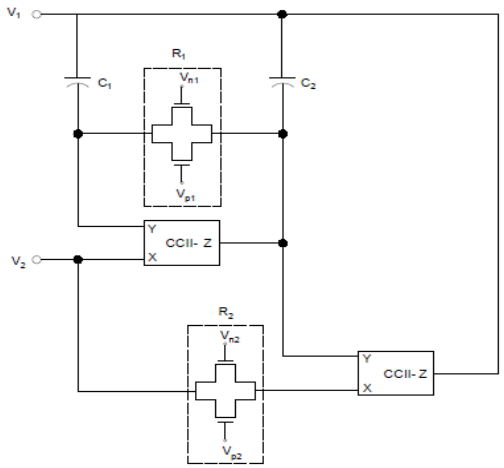

Fig. 3. The FDNR circuit

The FDNR is a circuit element that exhibits a purely real negative resistance that decreases in magnitude at a rate of -40 dB/decade. It is usually implemented from a generalized impedances convertor (GIC) or gyrator.

$$Z = \frac{1}{s^2KC} = -\frac{1}{\omega^2KC} \qquad (2)$$

Here passive resistors are replaced by MOS resistors. The linear region can be obtained by varying the control voltage V_n [15]. Here the analysis shows that the property of nonlinearity for every transistor, that will be cancelled by its counterpart [13]. After that we get a conclusion about the linear programmable resistor is to be found and given by:

$$R = \frac{(V_1 - V_2)}{I}$$
$$= \frac{1}{K_0(V_n - V_p - V_{tn} + V_{tp})} \qquad (3)$$

Where K_0 is the transconductance of the transistor and V_t is the threshold voltage. Equation (3) shows that R is a linear resistor and that can be controlled by voltages V_n or V_p. In this case V_p is to be fixed at -0.9V where as V_n is control the current entering in this configuration to make resistance of MOS to be constant.

III. LADDER BAND PASS FILTER OF SIXTH ORDER

The ladder band pass filter of sixth order as realized shown below using current conveyors as shown below in Fig. 4. With the help of passive elements as inductors, capacitors and resistors [11]. The equivalent transfer function is of the ladder band pass filter is shown below equation:

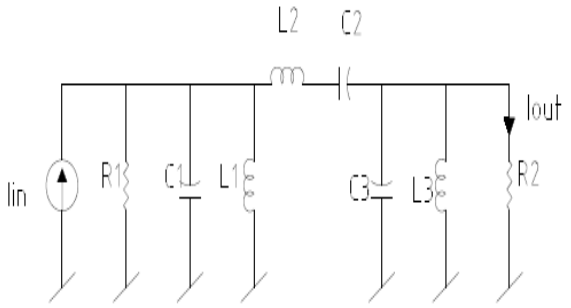

Fig. 4. A Ladder Band Pass Filter of Sixth Order

The equivalent circuit of the ladder filter using FDNR and passive components is shown below in Fig. 5.

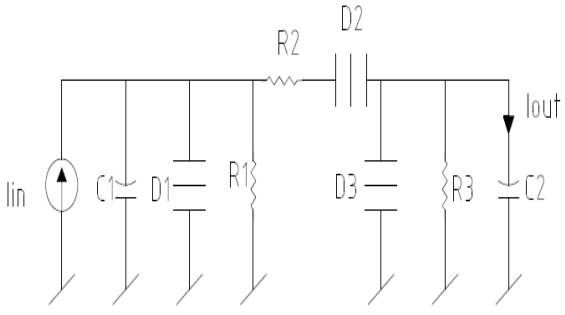

Fig.5. Equivalent Ladder Filter using FDNR

$$\frac{I_{out}}{I_{IN}} = \frac{C_2L_1L_3R_1S^3}{R_1R_2+s(L_3R_1+L_1R_2)+s^2(L_1L_3+C_1L_1R_1R_2+C_2L_1R_1R_2+C_2L_2R_1R_2+C_2L_3R_1R_2+C_3L_3R_1R_2)+s^3(C_1L_1L_3R_1+C_2L_1L_3R_1+C_2L_2L_3R_1+C_2L_1L_2R_2+C_2L_1L_3R_2+C_3L_1L_3R_2)+s^4(C_2L_1L_2L_3+C_1C_2L_1L_2R_1R_2+C_1C_2L_1L_3R_1R_2+C_1C_3L_1L_3R_1R_2+C_2C_3L_1L_3R_1R_2+C_2C_3L_2L_3R_1R_2)+s^5(C_1C_2L_1L_2L_3R_1+C_2C_3L_1L_2L_3R_1R_2)+s^6C_1C_2C_3L_1L_2L_3R_1R_2)}$$

After transformation of the ladder filter the element values are selected as below: $C_S=C_L=1.6pF$, $R_1=658\Omega$, $R_2=478\Omega$, $R_3=295\Omega$, $D_1=C_{X1}C_{X2}R_X$ where $C_{X1}=C_{X2}=29pF$, $R_X=R_{X1}=R_{X2}=325\Omega$, $D_2=C_{Y1}C_{Y2}R_Y$ where $C_{Y1}=C_{Y2}=1.2pF$, $R_Y=R_{Y1}=R_{Y2}=558\Omega$, $D_4=C_{Z1}=C_{Z2}=6.8pF$, $R_Z=R_{Z1}=R_{Z2}=229$

Table 1: Aspect ratios of MOSFETs used in CCII- are as follows:

Transistor Name	W	L
NMOS		
M1A	49.2µm	0.36µm
M2A	23.5µm	0.36µm
M6A	36µm	0.36µm
M10A	30µm	0.36µm
M11A	45µm	0.36µm
M12A	56µm	0.36µm
M13A	30µm	0.36µm
M1B	115.7µm	0.36µm
M2B	46.1µm	0.36µm
M6B	250µm	0.36µm
M10B	119.5µm	0.36µm
M11B	2µm	0.36µm
M12B	33.2µm	0.36µm
M13B	32µm	0.36µm
PMOS		
M3A	128µm	0.36µm
M4A	115µm	0.36µm
M5A	105µm	0.36µm
M7A,M8A	120µm	0.36µm
M9A	121µm	0.36µm
M3B	10µm	0.36µm
M4B	65µm	0.36µm
M5B	51µm	0.36µm
M7B	30µm	0.36µm
M8B	52µm	0.36µm
M9B	109µm	0.36µm

Table 2: W/L ratio of MOSFETs used in CMOS voltage control resistors are as follows:

Transistor Name	W	L
NMOS		
Mxn1	75µm	0.36µm
Mxn2, Myn1, Myn2, Mrn1	36 µm	0.36µm
Mzn1	35 µm	0.36µm
Mzn2	85 µm	0.36µm
Mrn2, Mrn3	25 µm	0.36µm
PMOS		
Mxp1	48 µm	0.36µm
Mxp2	31 µm	0.36µm
Myp1	30 µm	0.36µm
Myp2	26 µm	0.36µm
Mzp1	40 µm	0.36µm
Mzp2	35 µm	0.36µm
Mrp1	30 µm	0.36µm
Mrp2	28 µm	0.36µm
Mrp3	40 µm	0.36µm

Table 3: Level 7 SPICE parameter for 0.18µm CMOS process is as below:

.MODEL CMOSN NMOS (LEVEL = 7 +VERSION = 3.1 TNOM = 27 TOX = 4E-9 XJ = 1E-7 NCH = 2.3549E17 VTH0 = 00.3662648 K1 = 0.5802748 K2 = 3.124029E-3 K3 = 1E-3 K3B = 3.3886871 W0 = 1E-7 NLX = 1.766159E-7 +DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 1.2312416 DVT1 = 0.3849841 DVT2 = 0.0161351 U0 = 265.1889031 UA = -1.506402E-9 +UB = 2.489393E-18 UC = 5.621884E-11 VSAT = 1.017932E5 A0 = 2 AGS = 0.4543117 B0 = 3.433489E-7 B1 = 5E-6 KETA = -0.0127714 +A1 = 1.158074E-3 A2 = 1 RDSW = 136.5582806 +PRWG = 0.5 PRWB = -0.2 WR = 1 WINT = 0 +LINT = 1.702415E-8 XL = 0 XW = -1E-8 DWG = -4.211574E-9 DWB = 1.107719E-8 VOFF = -0.0948017 NFACTOR = 2.1860065 CIT = 0 +CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 +ETA0 = 3.335516E-3 ETAB = 6.028975E-5 +DSUB = 0.0214781 PCLM = 0.6602119 +PDIBLC1 = 0.1605325 PDIBLC2 = 3.287142E-3 +PDIBLCB = -0.1 DROUT = 0.7917811 PSCBE1 = 6.420235E9 PSCBE2 = 4.122516E-9 PVAG = 0.0347169 DELTA = 0.01 RSH = 6.6 MOBMOD = 1 PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 +KT2 = 0.022 UA1 = 4.31E-9 UB1 = -7.61E-18 +UC1 = -5.6E-11 AT = 3.3E4 WL = 0 WLN = 1 +WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 +LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 +XPART = 0.5 CGDO = 8.06E-10 CGSO = 8.06E-10 CGBO = 1E-12 CJ = 9.895609E-4 PB = 0.8 MJ = 0.3736889 CJSW = 2.393608E-10 +PBSW = 0.8 MJSW = 0.1537892 CJSWG = 3.3E-10 PBSWG = 0.8 MJSWG = 0.1537892 CF = 0 PVTH0 = -1.73163E-3 PRDSW = -1.4173554 +PK2 = 1.600729E-3 WKETA = 1.601517E-3 +LKETA = -3.255127E-3 PU0 = 5.2024473 +PUA = 1.584315E-12 PUB = 7.446142E-25 +PVSAT = 1.686297E3 PETA0 = 1.001594E-4 +PKETA = -2.039532E-3)
.MODEL CMOSP PMOS(LEVEL = 7 +VERSION = 3.1 TNOM = 27 TOX = 4E-9 XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.3708038 K1 = 0.5895473 K2 = 0.0235946 K3 = 0 K3B = 13.8642028 W0 = 1E-6 NLX = 1.517201E-7 +DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 0.7885088 DVT1 = 0.2564577 DVT2 = 0.1 U0 = 103.0478426 UA = 1.049312E-9 UB = 2.545758E-21 UC = -1E-10 VSAT = 1.645114E5 +A0 = 1.627879 AGS = 0.3295499 B0 = 5.207699E-7 B1 = 1.370868E-6 KETA = 0.0296157 A1 = 0.4449009 A2 = 0.3 RDSW = 306.5789827 PRWG = 0.5 PRWB = 0.5

WR = 1 +WINT = 0 LINT = 2.761033E-8 XL = 0 XW = -1E-8 DWG = -2.433889E-8 DWB = -9.34648E-11 VOFF = -0.0867009 NFACTOR = 2 CIT = 0 +CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 +ETA0 = 1.018318E-3 ETAB = -3.206319E-4 +DSUB = 1.094521E-3 PCLM = 1.3281073 +PDIBLC1 = 2.394169E-3 PDIBLC2 = -3.255915E-6 PDIBLCB = -1E-3 DROUT = 0 +PSCBE1 = 4.881933E10 PSCBE2 = 5E-10 +PVAG = 2.0932623 DELTA = 0.01 RSH = 7.5 +MOBMOD = 1 PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9 UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 WL = 0 +WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 +CAPMOD = 2 XPART = 0.5 CGDO = 6.52E-10 CGSO = 6.52E-10 CGBO = 1E-12 CJ = 1.157423E-3 PB = 0.8444261 MJ = 0.4063933 +CJSW = 1.902456E-10 PBSW = 0.8 MJSW = 0.3550788 CJSWG = 4.22E-10 PBSWG = 0.8 +MJSWG = 0.3550788 CF = 0 PVTH0 = 1.4398E-3 PRDSW = 0.5073407 PK2 = 2.190431E-3 WKETA = 0.0442978 LKETA = -2.936093E-3 PU0 = -0.9769623 PUA = -4.34529E-11 PUB = 1E-21 PVSAT = -50 PETA0 = 1.002762E-4 PKETA = -6.740436E-3)

IV. SIMULATION RESULT

The result of band pass filter of sixth order is simulated in PSPICE tool. The filter is designed to provide a 40MHz cut-off of frequency. The result of the simulation for filter is shown in Fig. 6

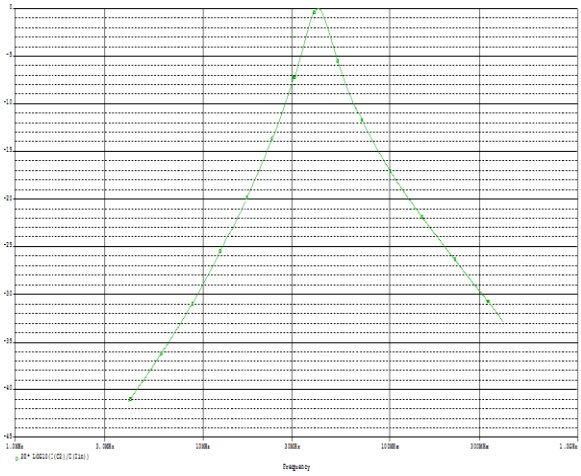

Fig. 6. CMOS based Current Conveyor Circuit

V. COMPARISON

The comparison between the previous published ladder filter with the new one designed ladder band pass filter of sixth order using FDNR is now in order. It is found to be the proposed circuit required of two MOS resistors having a nature to control the voltages according to the designer for tuning purpose, use of two floating capacitor (for IC implementation) and the voltages is to be at 1.25V. The previous is designed using the passive resistors as in the analog electronics, are very bulky in nature that's why use of active resistors removes the drawback of required elements in previous one.

VI. CONCLUDING REMARKS

An FDNR lossless circuit of floating type is having of two current conveyors of negative type (CCII-) and two passive capacitor and four MOS resistor components is to be used. The performance of FDNR is verified for ladder band pass filter of sixth order. The simulations of the circuit performed using 0.18µm CMOS technology parameters. The theoretical and simulation result has the good proximity. The main advantage of the modified circuit is the reduced in power consumption and the use of MOS-R makes the controlling of resistor by a suitable control voltage irrespective to physical passive resistor.

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