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Original Article

Retention Time Optimization In 3TDRAM Using Parametric Variation In Nanometer Regime

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Abstract *- Retention time play a very prominent role in dynamic random-access semiconductor memory. During the implementation of low power devices, VLSI designer faces the problem of leakage current, Small device geometry and minimum area utilization on a silicon wafer. Moore's law states that no of transistor doubles on a small portion of a silicon wafer after every two years. On a nanometer scale, CMOS technology has certain limitations due to the abrupt effect of small device geometry and leakage current. In this paper, analysis of leakage current and leakage power is done and mainly focus on improvement of retention time in 3TDRAM using leakage reduction finfet technology is proposed. Leakage reduction finfet technology is a leakage reduction schematic design in 3TDRAM that overcomes the issues related to traditional CMOS technology, and it does not require additional circuitry. Cmos and double gate finfet technology are proposed for implementation of 3TDRAM using cadence tool at 90nm technology. 3TDRAM is examined with Variation in supply voltage and capacitance value for CMOS and double gate finfet technology. As the results are compared, Retention time is more improved in double gate finfet technology as compared to CMOS technology is observed.*

Keywords - *Retention Time, Refresh frequency, Leakage Current, Leakage Power, Average Current, Average Power.*

I. INTRODUCTION

Since the invention of the mos transistor, Integrated circuit technology has progressed very rapidly. Recently various leakage reduction techniques have been reported to increase the retention time in dynamic random access memory. The rapid progress in an integrated circuit is achieved by scaling in mos devices. Transistor Scaling plays a vital role in shrinking the size of mos transistor. Miniaturization, the size of mos transistor, leakage parameters affect the performance of mos device. During the implementation of low power, electronic devices leakage parameters are the biggest challenge for VLSI circuit designers. 3TDRAM is implemented by different leakage reduction techniques using CMOS technology, but it has certain limitations. Hence to overcome the limitation and issues of CMOS technology, double gate finfet technology is introduced.

Finfet operation is very much similar to mosfet. But the use of double gate in finfet technology control the channel very effectively, which help for a reduction in leakage parameters and improvement in retention time. Scaling in planar mosfet technology reduces the device size and short channel effect (SCE) induced. Instead of CMOS technology, double gate technology is contingent on multiple gates devices having superior control over the short channel effect. Finfet technology, i.e. double gate mosfet, is a good option to overcome the problem of the short channel effect in planar mosfet. New innovations in VLSI design finfet technology are performing superior as compared to traditional CMOS technology. Double gate finfet technology is an additional compatible with existing CMOS technology.

II. RELATED WORK

Dynamic random access memory is the main or central memory system used in several electronic gadgets. In dram data storage on a capacitor in the form of a charge over it. But due to leakage in mos transistor, the stored charge on the capacitor decreases gradually, and there is a possibility of a loss of information or data. To prevent data loss, refresh operation play an important role, and it will affect reversely on system performance. To overcome the issues of leakage and refresh operation in dram finfet technology is introduced.

Leakage is a major issue in 3T dynamic random access memory. In semiconductor memory, off-state current contributes power dissipation in mos devices. 3T dynamic random access memory is implemented with finfet technology to minimize leakage parameters are examined. 3T DRAM with finfet circuit design provides better results as compared to traditional 3T DRAM circuit design [1]. Implementation of a dram with finfet technology affects on dram cell behaviour was proposed. Dram cell is implemented by planar CMOS, finfet and III-IV mosfet for various reliability scenarios, i.e. variability and soft error. Finfet based circuit provides good results as compared to other devices [2].In the L1 memory cache, six transistors are replaced by a 3T1D cell for device variability issues [3]. A charge injection device has been made for high density dynamic random access memories. It required minimum area as compared to traditional transistors [4]. Performance of integrated circuits implemented by CMOS degenerates by short channel effect and leakage current. Leakage current contributes maximum power dissipation

in an integrated circuit were implemented by CMOS. Digital circuits are implemented by CMOS, and finfet technology and performance are measured in terms of power dissipation and delay. Finfet technology provides a better result as compared to traditional CMOS technology was proposed [5]. Here the implementation of 3T dram and 4T dram using carbon nanotube field-effect transistor (CNTFET) for investigation of leakage parameters and delay time was proposed. The 3T dram has minimum leakage power and power dissipation than the 4T dram. But 3T DRAM having more delay compared to 4T dram was proposed [6]. Implementation of 3T1D dram and modified 3T1D dram was carried out for investigation of various leakage parameters. Power consumption and access time in modified 3T1D dram was minimum investigated. Retention time improvement is slightly achieved in modified 3T1D dram design [7]. Comparative analysis of CMOS, soi and finfet technology is done [8]. Power dissipation analysis in 3T and 4T dram memory for different nanometer regimes are examined. In semiconductor memories, off state (I_{off}) leakage current cause power dissipation. At 45nm technology, average power dissipation is lesser in 3T as compared to 4T [9]. As shrinking the size of mos device, finfet technology is the best option for planar mosfet. In double-gate finfet technology, the gate controls the channels induced between source and drain appropriately. The intensity of leakages is minimized in finfet technology as compared to CMOS technology were proposed [10]. Data stability is a prominent parameter is static random access memory. The memory array is also a prominent source of leakage in memories. In semiconductor memories, improvement of data stability and memory density achieved by reducing active and standby power with independent gate finfet technology was proposed [11]. As the device was scaled down more and more, leakage reduction and reduction in a device to device variability were more challenging. Finfet is the superior technology as compared to conventional CMOS technology for enhancement in leakage reduction and device to device variability [12]. Retention Time and refresh frequency are the parameters considered for performance measurement in dynamic random access memory. Variations in parameter value affect the retention time and refresh frequency were examined. As the retention time was affected by leakage issue in mos transistor, the corresponding degradation of performance of dynamic random access memory was observed [13].In semiconductor memory, performance was degraded by the influence of leakage current. There are multiple sources of leakage in mos transistors. Leakage current analysis was done using 1T1C DRAM by Variation of parameters value as the capacitance value increases leakage parameters decreases. Similarly, Variation in supply voltage increases the leakage parameters to a great extent was proposed [14]. Subthreshold current play a major role in mos transistor leakage current when $V_{gs}<V_{th}$. Subthreshold characteristics are examined by the difference between top and bottom flat band voltage with Variation of dielectric constant. By Variation in a difference between top and bottom flat band voltage with Variation of dielectric constant, Threshold voltage remains constant but on-off current ratio increases were observed [15]. Low power circuit design trends are increasing day by day in the daily need of life. To design low power devices, threshold voltage was the adjusting parameter to operate the device in the weak inversion region were proposed. Low power memory design techniques were proposed [16]. Parasitic effect in Nanoscale technology of VLSI affects the system performance. Instead of traditional mosfet, a different doping profile in mosfet considered for low power application with minimum leakage parameters in VLSI design is proposed [17].

III. 3T DRAM CELL AND EXPERIMENTATION

A. 3T DRAM CELL CIRCUIT DIAGRAM

All 3TDRAM consists of three transistors, M_1, M_2 and M_3, respectively. Input or output line can be Bit line and bit line bar. Read and write act as word lines to turn on and off the respective transistor. C_1 and C_2 are precharge capacitors, and C_s is the storage capacitor. During a write operation, W=1, R=0, M_1=on, and M_2=M_3=off, C_1 is a precharge capacitor to V_{dd}, Bit line(B_L) treated as an input. When bit line(B_L) =1, the voltage that appears across the storage capacitor is "V_{dd}-V_{tn}".

When bit line(B_L) =0, the voltage that appears across the storage capacitor is 0v.

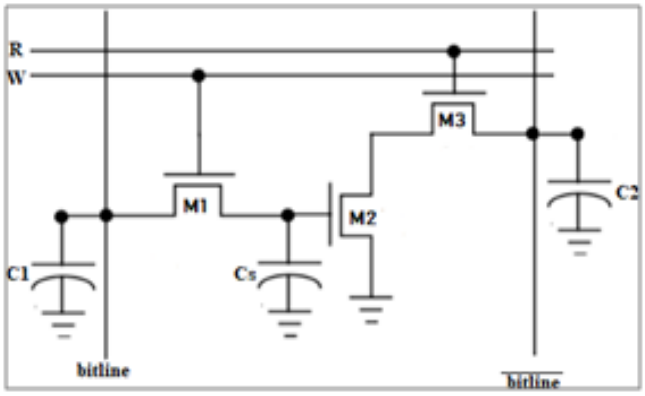

Fig 1 3T Dynamic random access memory

During a read operation, R=1, W=0, M1=off, and M_3=on, C_2 is a precharge capacitor to V_{dd}. The voltage appears across the storage capacitor as "V_{dd}-V_{tn}" it will turn on transistor M_2. If M_2 and M_3 both turn on, the voltage at precharge capacitor C_2 is reduced. Therefore voltage appearing at the bit line bar is 0v, and it will sense by the sense amplifier, and output is 1.

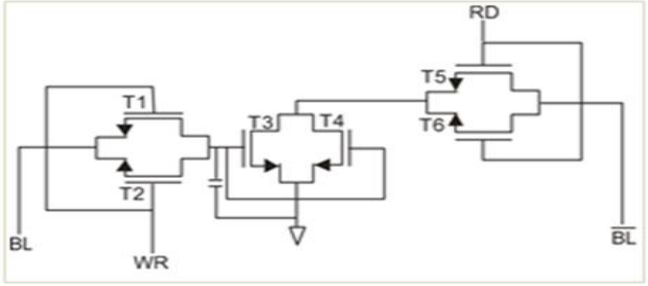

Fig 2 3TDRAM with Finfet

If voltage appears across storage capacitor is 0v, it will turn off transistor M_2. If M_2 is off and M_3 is on, the voltage at precharge capacitor C_2 is V_{dd}. Therefore voltage appearing at the bit line bar is 1v, and it will sense by the sense amplifier, and output is 0.

B. Performance Measuring Parameters

For the performance evaluation, Analysis of leakage parameters has been carried out and examined Variation of retention time and refresh frequency. The mathematical representation or expressions of the performance measuring parameters are given below.

a) Sub-threshold Leakage Current

The main cause of sub-threshold leakage current is, $V_{gs}<V_{th}$ of mos transistor. During this case, the mos transistor operates in a weak inversion region, and it is in an off state[13]. The sub-threshold leakage current mathematically expressed as

$$I_{subthreshold} = I_0 e^{\frac{(Vgs-Vth)}{nV_T}} [1-e^{-(\frac{V_{ds}}{V_T})}] \ldots\ldots(1)$$

Where,

$$I_0 = \frac{W \mu_0 C_{OX} V_T^2 e^{1.8}}{L},$$

$$V_T = \frac{KT}{q} = \text{Thermal voltage},$$

V_{th} = Threshold voltage(Volt),
V_{ds} = Drain to source voltage(Volt),
V_{gs} = Gate to source voltage(Volt),
C_{ox} = Gate oxide capacitance(F/m2),
μ_0 = Carrier mobility,
n = Sub-threshold swing coefficient.
L = Transistor Length(nm)
W = Transistor Width(nm) [1][13].

b) Leakage Power

The size of the mos transistor is minimized by scaling techniques. As the device size reduces power dissipation in devices contributes to leakage power. In mos device leakage power is given by[13]

$$P_{Leak} = I_{Leak} * V_{dd} \ldots\ldots\ldots(2)$$

Where,
P_{Leak}= Leakage power,
I_{Leak} = Leakage current,
V_{dd} = DC Power supply.

c) Retention Time or Holding Time(T_h)

Retention time plays a very important role in semiconductor memory during charge storing on the storage capacitor. It is the longest period of time that the cell can maintain a large enough voltage to be interpreted as logic 1 or high voltage. Retention Time is given by

$$\text{Retention Time} = T_h = \Delta t = [C_S/I_L] * \Delta V_S \ldots\ldots\ldots(3)$$

Where,
C_s= Storage Capacitor
I_L= Leakage Current
Δt and ΔV_S represent Changes in time and supply voltage

Holding time or Retention Time may be increased by using large capacitance and minimizing the leakage current.

d) Refresh Frequency ($F_{refresh}$)

DRAM cell must behold data as long as the charge on the storage capacitor is maintained. To overcome the leakage problem, the dram cell must be refreshed periodically. The refresh frequency is given by

$$F_{Refresh} = [1/2T_h] \ldots\ldots\ldots\ldots(4)$$

Where
T_h=Retention Time or Holding Time

C. 3TDRAM schematic Diagram

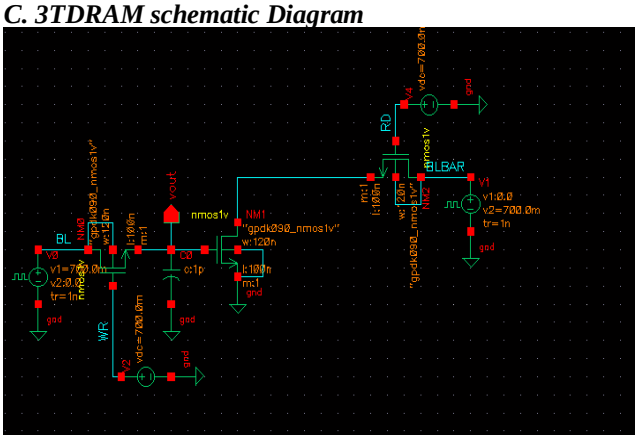

Fig. 3 3TDRAM Schematic Diagram

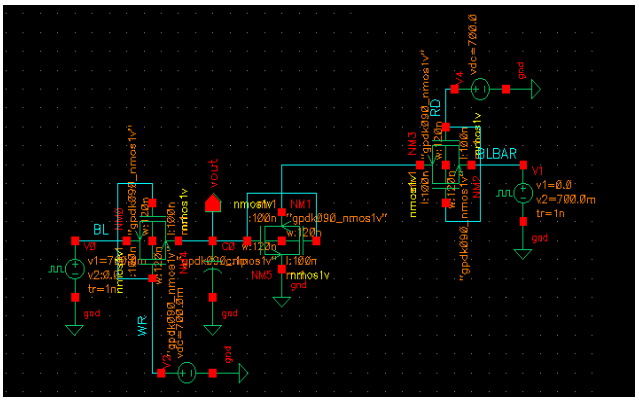

Fig. 4 3TDRAM with Finfet Technology Schematic

D. Simulation of 3T DRAM Cell

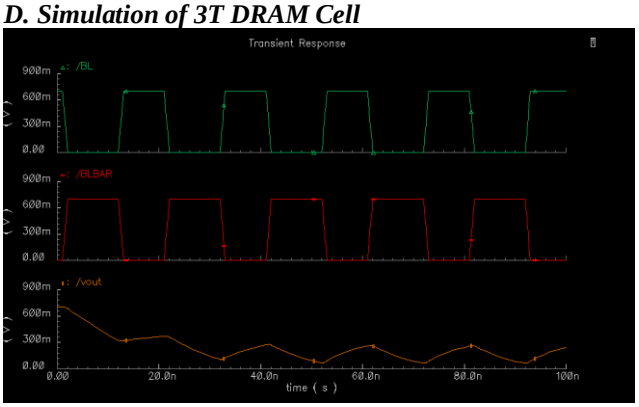

Fig. 5 3TDRAM Transient Response

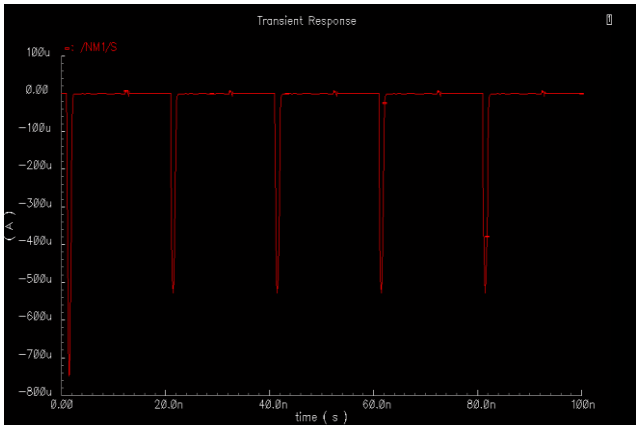

Fig. 6 3TDRAM Leakage current

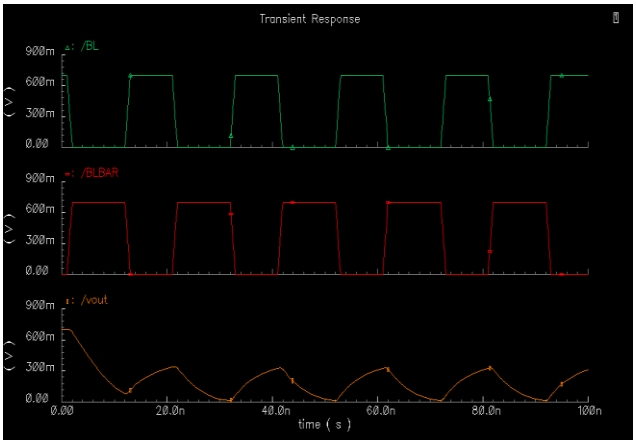

Fig. 7 3TDRAM with finfet transient response

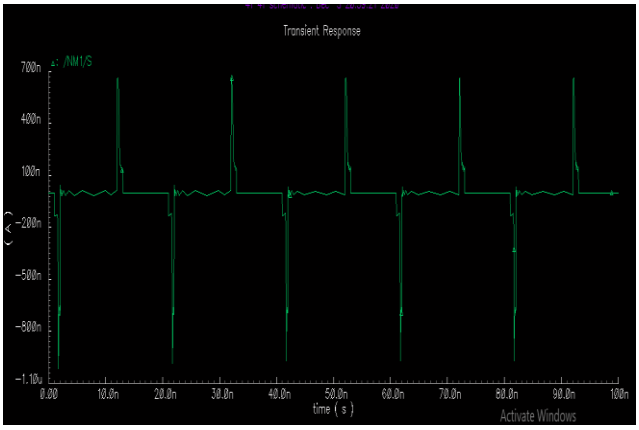

Fig. 8 3TDRAM with finfet Leakage current

IV. RESULTS AND DISCUSSION

In this work, 3T DRAM is implemented and simulated by conventional CMOS technology and leakage reduction double gate finfet technology. In both, cases leakage parameters and retention time are analysed by Variation of supply voltage and storage capacitance value. The simulation results of CMOS and finfet technology are shown in Table I and Table II, respectively. Leakage current observed maximum in CMOS technology as compared to finfet technology by Variation of the supply voltage. Leakage power observed maximum in CMOS technology as compared to finfet technology by Variation of the supply voltage. Retention time observed maximum in finfet technology as compared to CMOS technology by Variation of the supply voltage.

Variation in storage capacitance value minimized the leakage current in finfet technology as compared to CMOS technology and observed that retention time improvement was achieved to a great extent using finfet technology. Due to improvement in retention time, refresh frequency goes down.

Table 1

PART A: 3TDRAM CMOS Technology							
Case1: Supply Voltage Variation [Technology=90nm,W=120nm,L=100nm,Cs=1pF]							
Sr. No.	**Supply Voltage (V)**	**Leakage Current (uA)**	**Leakage Power (uW)**	**Average Current (uA)**	**Average Power (uW)**	**Retention Time (Th) (ns)**	**Refresh Frequency (Frefresh) (Khz)**
1	0.5	1.3	6.8	9.9	4.95	384.61	1300
2	0.7	2.2	6.1	11.6	8.12	318.18	1570
3	1	2.7	2.7	15.8	15.8	370.37	1350
4	1.2	3.6	4.3	16.5	19.8	333.33	1500
5	1.5	5	7.5	17.6	26.4	300	1660
Case 2: Capacitor Value Variation [Technology=90nm,W=120nm,L=100nm,Supply Voltage=0.7V]							
Sr.	**Capacit**	**Leakage**	**Leakag**	**Average**	**Average**	**Retention**	**Refresh Frequency**

No.	or Value (pF)	Current (uA)	e Power (uW)	Current (uA)	Power (uW)	Time (Th) (ns)	(Frefresh) (Khz)
1	1	2.2	6.1	11.6	8.12	318.18	1570
2	2	1.8	1.2	11.01	7.707	777.77	642.86
3	3	1.6	1.18	11.04	7.728	1312.5	380.95
4	4	1.2	0.9	11.08	7.756	2333.3	214.28
5	5	0.6	0.8	11.03	7.721	5833.3	85.71

Table 2

PART B:3TDRAM with DG FINFET Technology							
Case 1: Supply Voltage Variation [Technology=90nm, W=120nm, L=100nm, Cs=1pF]							
Sr. No.	**Supply Voltage (V)**	**Leakage Current (uA)**	**Leakage Power (uW)**	**Average Current (uA)**	**Average Power (uW)**	**Retention Time(Th) (ns)**	**Refresh Frequency (Frefresh) (Khz)**
1	0.5	0.1	0.08	5.4	2.7	5000	100
2	0.7	0.2	0.1	6.6	4.62	3500	142.85
3	1	0.6	0.6	8.9	8.9	1666.66	300
4	1.2	0.78	0.7	10.1	12.1	1538.46	325
5	1.5	1.23	0.98	10.8	16.2	1219.51	410
Case 2: Capacitor Value Variation [Technology=90nm, W=120nm, L=100nm, Supply Voltage=0.7V]							
Sr.No.	**Capacitor Value (pF)**	**Leakage Current (uA)**	**Leakage Power (uW)**	**Average Current (uA)**	**Average Power (uW)**	**Retention Time (Th) (ns)**	**Refresh Frequency (Frefresh) (Khz)**
1	1	0.2	0.1	6.6	4.62	3500	142.85
2	2	0.08	0.076	6.2	4.34	17500	28.57
3	3	0.06	0.054	5.8	4.06	35000	14.28
4	4	0.044	0.036	5.4	3.78	63636.36	7.85
5	5	0.032	0.022	5.1	3.57	109375	4.57

The graph points out that by Variation in supply voltage, the value of leakage current increases. From this graph, it is clear that the leakage current in CMOS technology obtained is higher than FINFET Technology is shown in Fig.9.

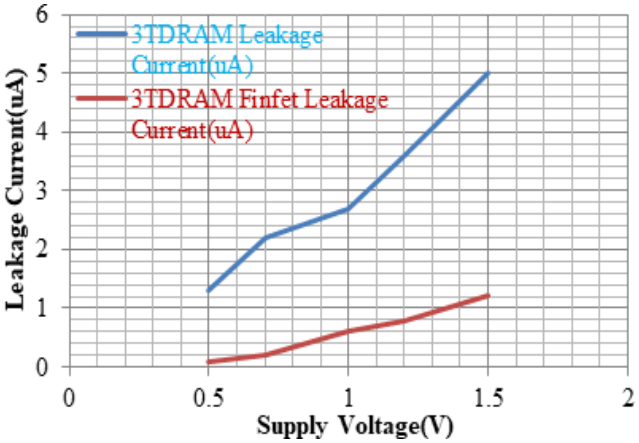

Fig. 9 Supply Voltage Vs 3TDRAM Leakage Current and 3TDRAM Finfet Leakage Current

The graph indicates that by Variation in supply voltage, the leakage power is increasing. From this graph, it is obvious that the leakage power in CMOS technology is obtained higher than FINFET Technology is shown in Fig.10.

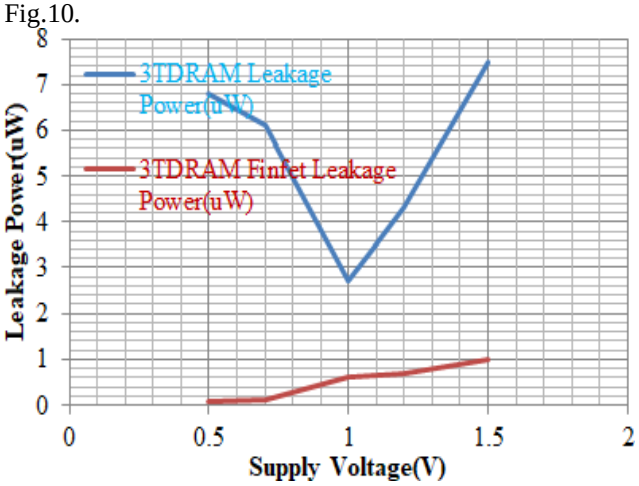

Fig. 10 Supply Voltage Vs 3TDRAM Leakage Power and 3TDRAM Finfet Leakage Power

Fig.11 shows a graph indicating that by Variation in supply voltage, the average current is increased. From this graph, it is clear that the average current in CMOS technology is obtained higher than in FINFET Technology.

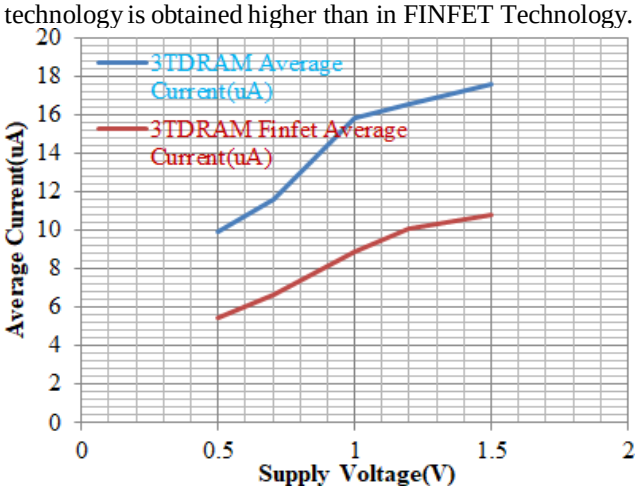

Fig. 11 Supply Voltage Vs 3TDRAM Average Current and 3TDRAM Finfet Average Current

Fig.12 shows a graph specifying that by Variation in supply voltage, the average power is increased. From this graph, it is clear that the average power in CMOS technology is obtained higher than in FINFET Technology.

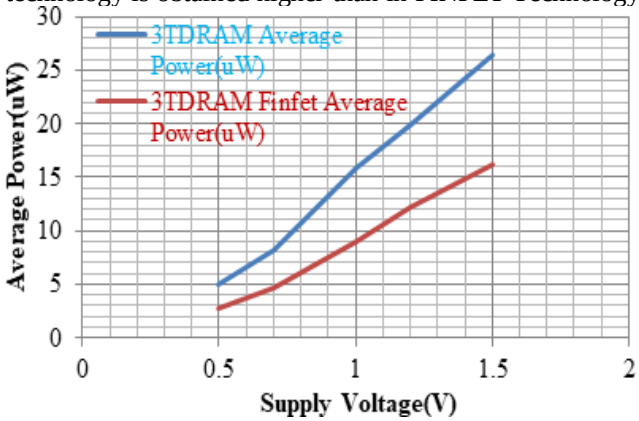

Fig. 12 Supply Voltage Vs 3TDRAM Average Power and 3TDRAM Finfet Average Power

From Fig.13, the graph indicates that the retention time improves in FINFET technology as compared to CMOS Technology.

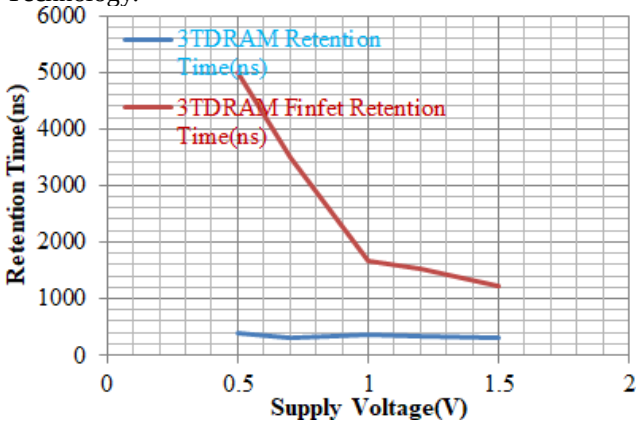

Fig. 13 Supply Voltage Vs 3TDRAM Retention Time(Th) and 3TDRAM Finfet Retention Time(Th)

Fig.14 shows graph indicates that by Variation in supply voltage, the Refresh Frequency is increased. From this graph, it is clear that the Refresh Frequency in CMOS technology is obtained higher than FINFET Technology.

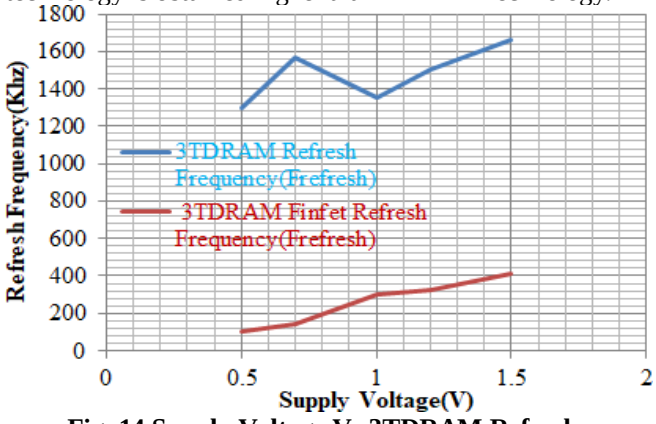

Fig. 14 Supply Voltage Vs 3TDRAM Refresh Frequency(Frefresh) and 3TDRAM Finfet Refresh Frequency(Frefresh)

Fig.15 shows graph indicates that by Variation the capacitor value, the leakage current is decreased. From this graph, it is clear that the leakage current in CMOS technology is obtained higher than in FINFET Technology.

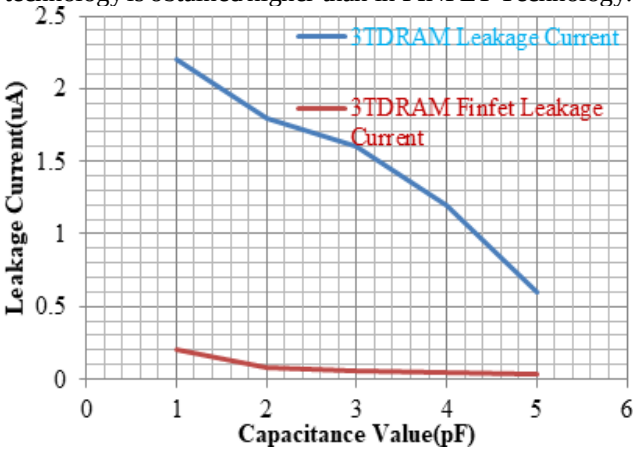

Fig. 15 Storage Capacitance Vs 3TDRAM Leakage Current and 3TDRAM Finfet Leakage Current

Fig.16 shows graph indicates that by Variation the capacitor value, the leakage power is decreased. From this graph, it is clear that the leakage power in CMOS technology is obtained higher than FINFET Technology.

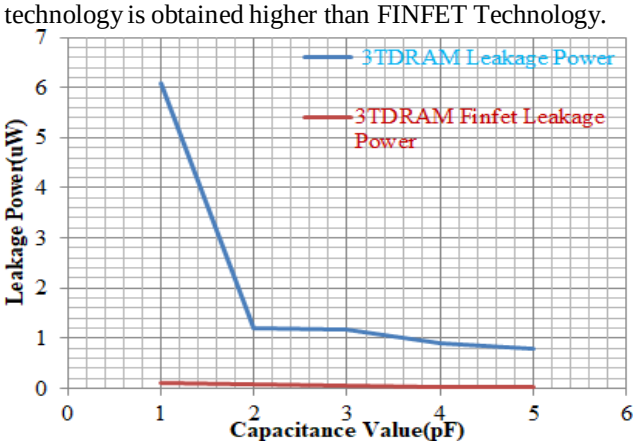

Fig. 16 Storage Capacitance Vs 3TDRAM Leakage Power and 3TDRAM Finfet Leakage Power

The graph points out that by Variation in capacitor value, the Average current is reduced. From this graph, it is clear that the Average current in CMOS technology is achieved higher than FINFET Technology is shown Fig.17.

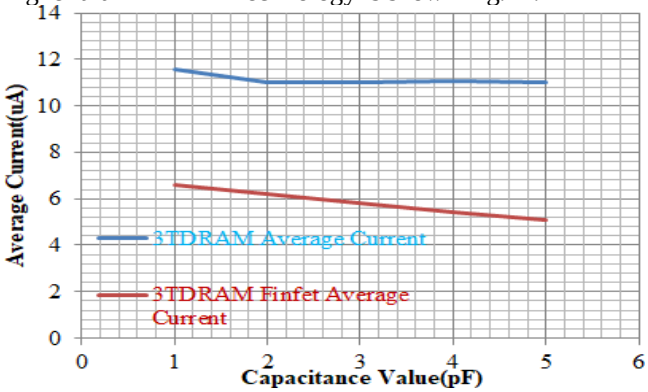

Fig. 17 Storage Capacitance Vs 3TDRAM Average Current and 3TDRAM Finfet Average Current

The graph points out that by Variation in capacitor value, the Average power is reduced. From this graph, it is clear that the Average power in CMOS technology is achieved higher than FINFET Technology is shown Fig.18.

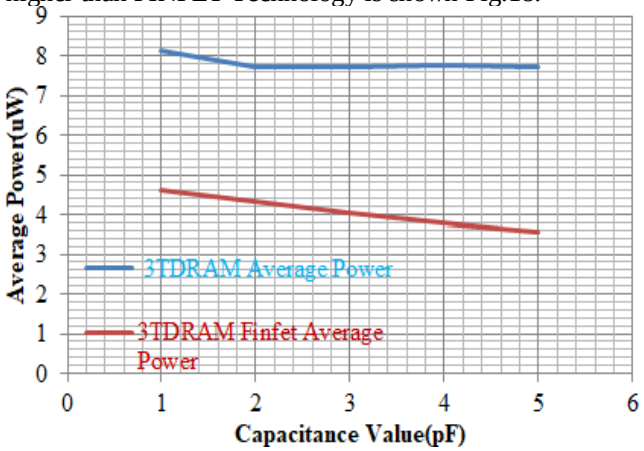

Fig. 18 Storage Capacitance Vs 3TDRAM Average Power and 3TDRAM Finfet Average Power

From Fig.19, the graph indicates that the retention time improves in FINFET technology as compared to CMOS Technology.

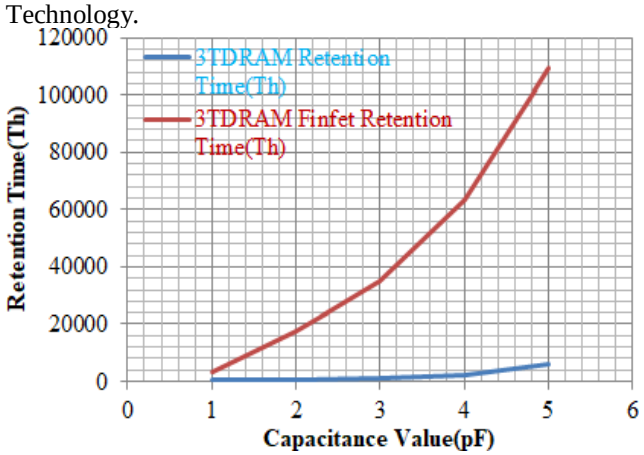

Fig. 19 Storage Capacitance Vs 3TDRAM Retention Time(Th) and 3TDRAM Finfet Retention Time(Th)

The graph points out that by Variation in capacitor value, the Refresh Frequency is reduced. From this graph, it is clear that the Refresh Frequency in CMOS technology is achieved higher than FINFET Technology is shown Fig.20.

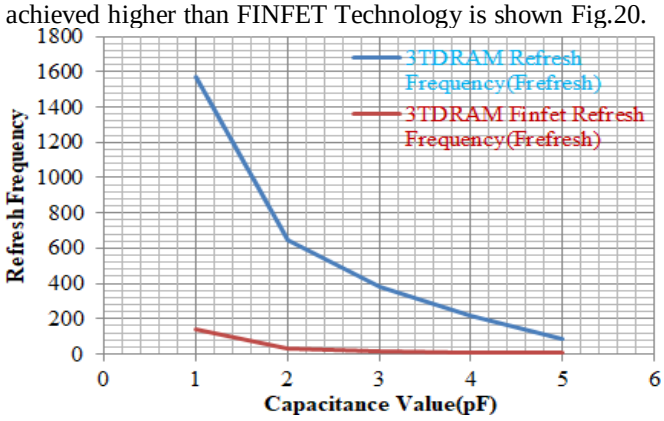

Fig. 20 Storage Capacitance Vs 3TDRAM Refresh Frequency(Frefresh) and 3TDRAM Finfet Refresh Frequency(Frefresh)

V. CONCLUSION

Development in VLSI technology offers the expanding requirement of large storage space capability instantly in the direction of the memory supported device. Day by day, the technology scales down, and then the requirement increases the devices have compact with low-level leakage current as well as lower supply voltage. To examine and calculate all the parameters by using finfet based 3T DRAM technology minimized leakage current (I_L), leakage power(P_L), average current(I_{avg}), average power(P_{avg}), and refresh frequency ($F_{refresh}$), Correspondingly retention time enhancement is observed. The intention of the proposed work is to investigate the leakage parameter, retention time or holding time and refresh frequency in 3TDRAM by Variation of parameter values. Circuit performance and accuracy is much more improved using finfet technology as compared to CMOS technology. The retention time obtained improved in finfet technology as compared to CMOS technology. It has been estimated that this finfet technology does not consume more area as well as provides improved values of retention time as compared to CMOS technology.

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