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Original Article

Design of Low Noise Amplifier using Particle Swarm-Based Shunt Feedback-Transformer Coupled Resonators for 5G Network

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Abstract - *The present 5G network demands speed, capacity, and reliability, and the imperative for high-performance components becomes paramount. At the heart of this mission is the Low Noise Amplifier (LNA), which plays a crucial role in keeping signals strong and clear while transferring data quickly. This paper introduces a novel approach of Particle Swarm-based shunt feedback -Transformer Coupled Resonators (PSbSF-TCR) to design LNA by integrating Particle Swarm Optimization (PSO) with Shunt Feedback and Transformer Coupled Resonators. Traditional LNAs struggle to balance low noise, high signal boost, and wide frequency range. Additionally, they cannot handle noise well initially and have a limited frequency range. The proposed method tries to overcome these challenges with a smart optimization technique called PSO to overcome the problems of old-fashioned methods. Here, it efficiently integrates Shunt Feedback into the proposed architecture to suppress noise at the input stage, while Transformer Coupled Resonators bolster selectivity and widen the operational bandwidth. This synergistic fusion of cutting-edge techniques empowers the proposed LNA to deliver unparalleled noise performance, gain, and bandwidth essential for 5G networks. Simulations validate the superior performance of the design, affirming its potential to catalyze the next phase of 5G network advancement, where signal integrity and bandwidth optimization are paramount.*

Keywords - *Low Noise Amplifier, Particle Swarm Optimization, Shunt Feedback and Transformer Coupled Resonators, PSbSF-TCR, 5G network.*

1. Introduction

5G technology has ushered in a new era of high-speed, low-latency wireless communication, offering unprecedented connectivity and data transfer capabilities [1]. Central to this progress is the use of millimeter-Wave (mmWave) frequencies (24 GHz and above), which unlock vast bandwidths to support diverse 5G applications [2]. The Low Noise Amplifier (LNA) is vital in mmWave receiver front-ends, ensuring signal integrity and sensitivity [3]. Due to atmospheric absorption and high propagation losses at mmWave frequencies, advanced receiver front-end designs are required [4]. As the first stage in reception, the LNA mitigates thermal fluctuations and enhances overall sensitivity [5]. Research on 5G LNAs focuses on overcoming challenges in achieving high performance at mmWave frequencies [6], enabling higher data rates and more efficient communication [7]. LNAs are key to receiving weak signals and improving data throughput, especially in safety-critical applications like V2X communication [8]. Low power consumption remains a challenge in mobile devices, affecting energy efficiency and battery life. The cost of implementing mmWave technologies can also be significant [9]. Amplifier-introduced noise can degrade weak signals, making noise reduction essential [10]. This research aims to develop novel LNA architectures and topologies suited for 5G mmWave demands [11], considering low power, compact design, and standard compatibility [12]. Reducing noise figures helps preserve signal quality during amplification [13]. The mmWave band (above 24 GHz) enables higher data rates and bandwidth [14], supported by innovations like multi-band circuits [15], transformer-based injection techniques [16], MIMO [17], and OTA designs [18]. They often address individual performance aspects but fail to deliver a holistic solution that optimizes gain, noise figure, bandwidth, and power efficiency [10-14]. The research gap lies in the lack of an LNA design that achieves this balance in a cost-effective and integration-friendly manner that is suitable for 5G mmWave applications. This study proposes a Particle Swarm-based Shunt Feedback–Transformer Coupled Resonator (PSbSF-TCR) LNA architecture to address this gap. By combining shunt feedback with transformer-coupled resonators and leveraging Particle Swarm Optimization (PSO), the design enhances selectivity, suppresses noise, and improves impedance matching across a wider bandwidth. The PSO algorithm fine-tunes circuit parameters to achieve

optimal trade-offs, making the proposed LNA architecture well-suited for compact, high-performance 5G systems.

2. Related Works

Some recent literature works are mentioned below,

Du Preez et al. [14] examined SiGe and CMOS technologies in the context of millimeter-wave transceivers, focusing on their innovation and evolution to meet the growing demand for wideband, data-intensive connectivity. It includes reviewing spectrum allocation and regulatory challenges, discussing application-specific requirements for semiconductor technology, and comparing CMOS and SiGe BiCMOS processes. The analysis extends to various circuit implementations, ranging from passive components to integrated transceivers, emphasizing the challenges and design trends in millimeter-wave implementations. The primary drawback is that some extreme environments and sophisticated applications still favour GaAs and GaN due to their superior output power and noise figure performance despite the higher cost and complexity.

Chen et al. [19] employ a multi-layered computing architecture that integrates various technologies across wireless, optical, and edge cloud domains, supporting experimentation in a dense urban setting. It involves deploying programmable mmWave front ends at 28/60 GHz, USRP Software-Defined Radios (SDRs), and Xilinx RFSOC evaluation boards, enabling various experimental capabilities across different network stack layers. These components are integrated into COSMOS nodes with varying form factors-large, medium, and small-to accommodate different deployment scenarios and research requirements. Users can remotely access the testbed to conduct experiments, utilizing software and Application Program Interfaces (APIs) for hardware control; however, the complexity of integrating diverse hardware and software components can pose a challenge for seamless experimentation.

In 40 nm RFCMOS technology, Verma et al. [20] have unveiled a 28 GHz receiver front-end intended for millimeter-wave band wireless communication. In order to overcome the difficulty caused by the lower ratio of operating carrier frequency to unity current gain frequency of MOSFETs, the receiver implements a standard Gm-C filter, a Gilbert cell-based mixer with common gate transconductance stage, and a three-stage low noise amplifier with push-pull topology. A current bleeding technique uses PMOS transistors in a standard gate configuration and NMOS transistors as resistors to further enhance linearity and gain. Comparing these methods to state-of-the-art designs improves the receiver's linearity performance. The receiver uses 36.7 mW of power to obtain a conversion gain of 30.5 dB, a noise figure of 2.15 dB, and an IIP3 linearity value of -21.7 dBm. The performance of the suggested receiver is measured with the Figure of Merit (FOM), yielding a value of 0.27, indicating its effectiveness in achieving high gain, low noise, and improved linearity.

Zimmer et al. [21] delve into the significant role of Silicon-Germanium Heterojunction Bipolar Transistors (SiGe HBTs) and BiCMOS technology in the advancement of present and future millimeter-Wave (mmWave) systems. A collaborative group from various esteemed institutions across Europe highlights the capabilities of these technologies to meet the growing demands of high-frequency applications. It explores the performance characteristics, design considerations, and potential applications of SiGe HBTs and BiCMOS in the mmWave spectrum, which spans 30 GHz to 300 GHz. It draws upon cutting-edge research and development in academic and industrial settings, providing a comprehensive state-of-the-art overview. A potential drawback could be the limitations in achieving even higher frequency operation or power output compared to other compound semiconductor technologies. However, SiGe continues to be a cost-effective and highly integrated solution.

Wibisono et al. [22] introduce an innovative co-design approach for a Dual-Band Low-Noise Amplifier (DB-LNA) and a Dual-Band Band-Pass Filter (DB-BPF) tailored explicitly for Radio Navigation Aid (RNA) applications operating at 113 MHz and 332 MHz. The core novelty lies in the direct integration of the DB-LNA with the DB-BPF, effectively utilizing the DB-BPF to function as the Output Matching Network (OMN) of the DB-LNA. This co-design structure is evaluated using Z_{in} analysis, and the design procedure is systematically outlined in four stages: individual DB-BPF design, individual DB-LNA design, cascading the discrete DB-LNA and DB-BPF, and finally, the proposed co-design integration. The authors validate the accuracy of this integrated architecture through impedance characteristic (Z_{in}) analysis, S-parameter simulations, and measurement results. A significant advantage of this co-design is the reported reduction of passive components by 31.5%. However, a potential drawback of such tight integration could be increased complexity in independently tuning or optimizing the performance of either the LNA or the BPF after fabrication.

Bijari et al. [23] introduce a meticulously optimized design for an Ultra-Wideband (UWB) LNA operating across the 2.5-10.5 GHz frequency range, implemented in 180-nm and 65-nm RF-CMOS technologies. The design incorporates a novel input-matching network that leverages resistive-inductive feedback alongside a noise-cancelling technique, effectively achieving broadband impedance matching and a low noise figure. Current-reused architecture and inductive peaking techniques minimize power consumption while ensuring high and consistent gain. The optimization process for this UWB-LNA relies on heuristic multi-objective optimization algorithms, specifically the Inclined Planes System Optimization (IPO) and PSO, utilizing HSPICE and Cadence Spectre RF for simulation and design. The post-

layout simulation results demonstrate impressive performance metrics, including an input return loss (S11) below -10 dB, a flat power gain (S21) of 13.2±0.5 dB and 14±0.5 dB for the 180-nm and 65-nm technologies, respectively, and a noise figure consistently below 5 dB and 2.5 dB across the entire UWB spectrum for the respective technologies; however, it does not explicitly delve into the chip area occupied by the design, which could be a potential drawback in area-constrained applications. Martinez-Perez et al. [24] developed a fresh idea of Inductor less noise-cancelling CMOS, addressing the challenge of balancing performance parameters often conflicting requirements. LNA balances the performance of two transistor stages. Instead of using closed-form expressions or straightforward simulations, it visualizes the design parameters in a 2-dimensional space, allowing for optimization without compromising other specifications.

The CS-CG noise-cancelling LNA in 65-nm CMOS technology may be designed with a 3.7-dB noise figure, a 17-dB gain, and the necessary cut-off frequency through highly competitive post-layout simulations produced by this method, which also benefits from complete device models. It allows designers to observe the design span and achieve a more advantageous trade-off than approaches focusing on isolated design points. However, the contour map used in this methodology does not represent the gradient of the curves or the effect of scenario variables. Table 1 shows the Challenges of the existing method.

Table 1. Challenges of the existing method

S. No	Author name	Method	Advantage	Disadvantage
1	Du Preez et al. [14]	Integrated circuits of CMOS and SiGe BiCMOS	Si-based processes offer cost-effective solutions with good RF performance and integration potential.	RF CMOS nodes still lag behind bipolar devices offered in SiGe BiCMOS processes.
2	Chen et al. [19]	Open-access, customizable millimeter-wave software-defined radios	Best suited for mobile and stable situations.	The complexity of managing and integrating various components and technologies within COSMOS
3	Verma et al.[20]	RFCMOS technology	Obtained good gain of conversion.	It needs to improve its Figure of merit.
4	Zimmer, et al. [21]	BiCMOS technologies	Shown better performance.	High manufacturing costs also increase complexity in design.
5	Wibisono, et al. [22]	Band pass filter and dual-band low-noise amplifier	The reduction in passive components, smaller overall size, and improved performance	Increased complexity in design.
6	Bijari, et al. [23]	LNA with CMOS technology.	Ideal for applications requiring UWB receivers with low power and low noise.	More complexity
7	Martinez-Perez, et al. [24]	inductor-less noise-cancelling CMOS LNA	Less complexity with low-cost design.	High computation time.

While previous research has explored LNA architectures using BiCMOS, RFCMOS, and hybrid receiver designs [19–22], these solutions often optimize only individual parameters such as gain or noise figure, lacking a holistic approach that balances noise suppression, bandwidth, impedance matching, and gain in a compact, integration-friendly manner.

This work introduces a novel PSbSF-TCR architecture that presents several distinctive contributions compared to existing research. The proposed design uniquely integrates PSO with shunt feedback, aimed at input noise suppression, and transformer-coupled resonators, which enhance bandwidth-a combination not previously explored in the reviewed literature. PSO effectively addresses the limitations of manual or static tuning approaches found in earlier studies. Furthermore, the method provides enhanced bandwidth and selectivity, overcoming the narrow operational ranges typical of conventional designs and enabling wideband performance suitable for 5G mmWave applications. Improved impedance matching is achieved through transformer coupling and algorithmic tuning, ensuring signal integrity at high frequencies.

The compact and scalable architecture supports practical integration into next-generation mobile and V2X communication systems. Collectively, these innovations represent a substantial advancement over prior work in delivering a comprehensive and efficient LNA solution tailored to the rigorous requirements of modern mmWave systems.

Key points to the proposed work are listed below.

- Initially, it defines the specifications for the LNA, including the target frequency band, bandwidth, gain, noise figure, and other relevant parameters.
- Then, create the LNA circuit using the simulation tool. Include the LNA, matching networks, biasing circuits, and other required components.
- Moreover, a proposed method, Particle Swarm-based shunt feedback -Transformer Coupled Resonators (PSbSF-TCR), is developed.
- Transformer-coupled resonators achieve higher gain across the desired bandwidth compared to other techniques. It has high-performance and compact mm-wave receiver front-ends for 5G LNAs.
- A resonance circuit with parasitic capacitances is built to increase the voltage gain using the shunt feedback architecture. Because of its superior reverse isolation, the topology increased gain and enhanced stability.
- Then, extract the parasitic parameters of the components, transmission lines, and interconnects in the millimeter-wave circuit.
- Next, optimize the parameters and achieve the desired performance. This can involve adjusting component values, matching networks, or biasing conditions.
- Finally, the performances regarding gain, Noise figure, frequency, and Power consumption are evaluated.

3. System Model and Its Problems

Minimizing power consumption is essential for battery-operated devices. Designing low-power millimeter-wave LNAs that still meet performance specifications is a delicate balance. Achieving a low noise figure in millimeter-wave LNAs is crucial for maintaining signal quality. However, it becomes challenging as noise performance degrades at higher frequencies. Because millimeter-wave components are sensitive [1, 2] to environmental influences, it is crucial to guarantee the LNA's robustness and dependability throughout various operating circumstances. Designing circuits at millimeter-wave frequencies is inherently complex [23, 26], requiring specialized knowledge and tools. The intricacies of high-frequency design can lead to longer development times and increased design complexity. Achieving low power consumption while maintaining performance is a constant challenge, especially for battery-operated devices. Higher frequencies and advanced technologies may demand more power, impacting the system's efficiency. To address this, the proposed PSbSF-TCR architecture incorporates Particle Swarm Optimization (PSO), which efficiently navigates the complex, nonlinear design space to fine-tune critical parameters such as feedback resistance, transformer coupling, and resonator values. PSO enables automated multi-objective optimization, ensuring robust performance under tight mmWave constraints by balancing gain, noise figure, and bandwidth in a way that manual or static methods cannot achieve. Figure 1 shows the system model.

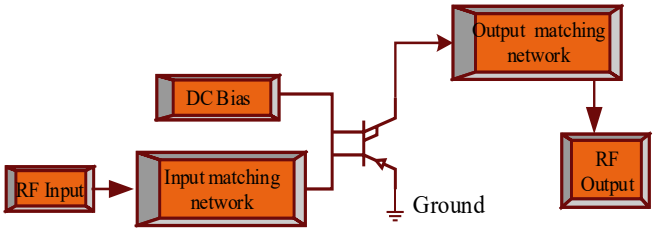


Fig. 1 System model and its problem

4. Methodology

This paper designs an optimized PSbSF-TCR topology operating at a millimetre-wave of the LNA model. The proposed method combines particle swarm optimization and shunt feedback topology with transformer-coupled resonators. PSO is used to optimize the matching network between the antenna and the LNA for efficient signal transfer and improved impedance matching, minimizing signal loss and reflections. Transformer-coupled resonators lead to higher gain across the desired bandwidth than other techniques. It has high-performance and compact mm-wave receiver front-ends for 5G LNAs. Transfer-coupled resonators can help achieve low noise figures, which is essential for maintaining good SNR. A resonant circuit with parasitic capacitances is built using the shunt feedback architecture to increase voltage gain. Because of its superior reverse isolation, the topology increased gain and enhanced stability. The architecture of the proposed PSbSF-TCR is given in Figure 2.

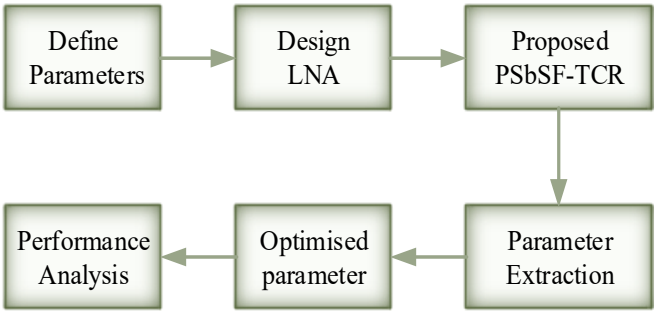


Fig. 2 Architecture of proposed PSbSF-TCR

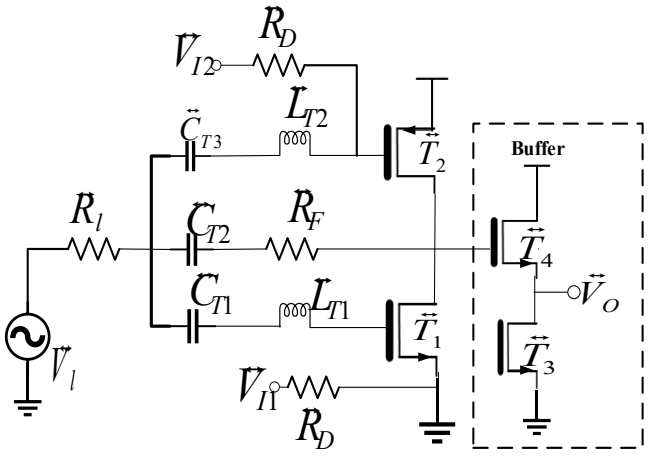


Fig. 3 Schematic diagram of proposed PSbSF-TCR topology

Moreover, Figure 3 demonstrates a circuit diagram of the LNA with a new design topology that uses peaking techniques. 45nm PSbSF-TCR topology with the decoupling capacitors$\vec{C}_{T1}$,$\vec{C}_{T2}$,$\vec{C}_{T3}$is the equivalent capacitance that represents the particle swarm optimization parameters inserted in the input matching network. The circuit topology enhances signal gain and suppresses input-referred noise.

Including feedback resistors and transformers helps achieve broadband impedance matching and improved linearity-the noises from the channel $\vec{T}_1$and$\vec{T}_2$resistor are placed in feedback$\vec{R}_F$. Voltages $\vec{V}_{I1}$and$\vec{V}_{I2}$ present in the design are to adjust gate voltage of$\vec{T}_1$and$\vec{T}_2$. $\vec{L}_{T1}$,$\vec{L}_{T2}$are the matching Inductor.$\vec{R}_D$and$\vec{R}_l$are the matching resistors. Transformer-Coupled Resonator provides wideband impedance transformation and efficient power transfer between cascaded stages. Using transformers minimizes parasitic effects and enhances gain across a broad frequency range. PSO tunes transformer turn ratios and coupling coefficients for optimal energy transfer. Moreover, the circuit design was conducted based on simulation results and the MATLAB model to reduce discrepancies between the design and measurements.

4.1. Design Parameters

Designing an LNA requires careful consideration of several critical parameters to ensure optimal performance within 5G networks, particularly in mmWave technology. These parameters include the frequency band of interest, specified gain requirements, noise figure, bandwidth, input/output impedance matching, power supply voltage and current, and technology constraints. The objective is to maximize signal strength and data capacity while minimizing unwanted noise. To achieve this, a formula called the biasing metricB_m has been devised, combining efficiency, gain, transit frequency, and minimum noise figure as expressed in Equation (1).

$$B_m = \frac{\left[\left(\frac{\vec{g}_c}{\vec{I}_R}\right)\bullet(\vec{g}_c/\vec{g}_{rs})\bullet(\vec{f}_{Tu})\right]}{min\left(\overleftrightarrow{NF}\right)} \quad (1)$$

So, to achieve high gain and bandwidth by reducing power consumption along with low noise figure, consideration is taken to the input design.

- The efficiency of transconductance$\vec{g}_c/\vec{I}_R$relates the $\vec{g}_c$transconductance of the transistor to the drain current$\vec{I}_R$, capturing the efficiency of the transistor.
- $\vec{g}_c/\vec{g}_{rs}$, represents the ratio of transconductance to output conductance, indicating the transistor's amplification capability.
- Unity gain frequency$\vec{f}T_u$ represents the frequency at which the transistor's current gain begins to roll off, influencing the circuit's bandwidth.

Maximizing$\vec{f}T_u$ the maximum amount of bandwidth while minimizing the noise figure$\overleftrightarrow{NF}$ is the goal of the biasing metric, which guides on achieving the highest overall efficiency while using the least amount of current. However, it also notes that trade-offs between frequency, noise figure, voltage gain, and power consumption can be made, especially as circuits move towards lower Integrated Circuits (ICs).

4.2. Design LNA

In order to design the LNA for broadband applications and to achieve low power and low voltage, shunt-based feedback is used. In contrast to conventional active load arrangements, this is accomplished by using a reusable current inverter, which essentially doubles the transconductance ($\vec{g}_c$) without resulting in any additional power consumption or output conductance degradation. This arrangement is depicted in Figure 4 below. The circuit uses two transistors with a feedback resistor connecting the output to the input gate. The resistor sets the input impedance, and the configuration enables current reuse, improving power efficiency. This approach supports input noise reduction and wideband impedance matching, making it suitable for mmWave LNA designs.

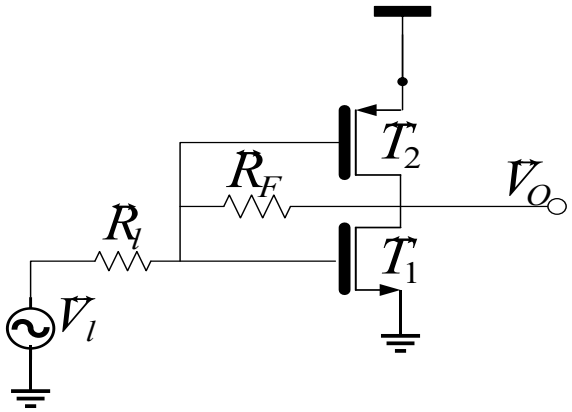


Fig. 4 Shunt-based resistive feedback to reuse current

The input impedance of a circuit can be calculated by considering the parallel combination of the input resistance and any reactive components present at the input. When a passive load with a resistive shunt feedback LNA, the input impedance can be approximated in Equation (2) using output resistance$\vec{R}_O$.

$$\vec{I}_{in} = \frac{\vec{R}_O+\vec{R}_F}{1+\vec{g}_c\vec{R}_O} \quad (2)$$

The amplifier's voltage gain is crucial for amplifying the signal while maintaining low noise. In a shunt series feedback LNA, the gain can be approximated by Equation (3).

$$\vec{A}_{Vg} = \frac{\vec{R}_O(1-\vec{g}_c\vec{R}_F)}{(\vec{R}_O+\vec{R}_F)} \quad (3)$$

The noise factor indicates the amount of noise the amplifier adds relative to an ideal noiseless amplifier. For a shunt series feedback LNA with a terminator, the noise factor at low frequencies can be approximated as given in Equation (4).

$$\overleftrightarrow{NF} \geq 1 + \frac{4\tau \vec{g}_c}{\phi \vec{R}_l}\left[\frac{(\vec{R}_O+\vec{R}_F)(\vec{R}_l+\vec{R}_F)}{(1-\vec{g}_c\vec{R}_F)\left(\vec{R}_O(1+\vec{g}_c\vec{R}_l)+(\vec{R}_l+\vec{R}_F)\right)}\right]^2 \quad (4)$$

Where$\phi = \left(\frac{\vec{g}_c}{\vec{g}_{DO}}\right)$ is the transconductance ratio, which is the fraction of the transconductance to the output conductance of the device, with an angular frequency w, and τ is the thermal noise coefficient, representing the noise generated internally within the device.

4.3. Proposed PSbSF-TCR

Inductive peaking is a technique used in electronic circuit design to compensate for the high-frequency roll-off in the gain response of amplifiers. The inductive series peaking network typically consists of an inductor in series with the feedback path as given in Figure 5. Since inductors and capacitors are connected in series, resulting in a resonance phenomenon at a specific frequency, they are also known as the Series resonators of LNA. This occurs to avoid the capacitance present in the gate-to-source, resulting from the overlap between the gate electrode and the drain and fringing fields. Moreover, Miller's effects on the capacitance between the gate and drain are effectively multiplied by the amplifier's voltage gain, leading to increased effective input capacitance and potentially reducing bandwidth. This configuration enhances selectivity and gain at the resonant frequency. The resistive feedback and load resistor contribute to wideband matching and output stability. The series Resonator sharpens the frequency response, improving gain at the center frequency while maintaining low insertion loss.

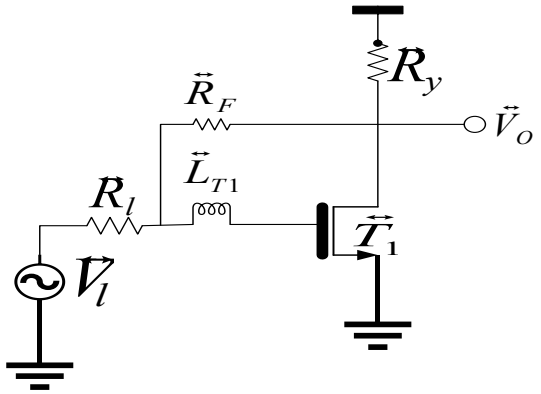


Fig. 5 Series resonators of LNA

The transconductance efficiency$\vec{g}_{c,eff}$ to LNA is given through the Equation (5). Here, this will represent the transconductance of the LNA with the combined effect of the peaking network.

$$\vec{g}_{c,eff} = \frac{\vec{g}_c}{\phi\left(1+\frac{\vec{R}_l}{\vec{R}_F}+\frac{\vec{R}_l}{\vec{R}_F^2}\vec{R}_a(\vec{g}_c\vec{R}_F-\phi)+\frac{jw\vec{C}_{as}\vec{R}_l}{\phi}\right)} \quad (5)$$

Where resistance in feedback$\vec{R}_a = \vec{R}_y // \vec{R}_F$, this enhanced transconductance can improve performance in specific applications, such as amplification or filtering, where maximizing $\vec{g}_c$ at particular frequencies is desirable.

Series Peaking in the Feedback is achieved by adding a capacitor in a specific part of the circuit to improve its ability to handle higher frequencies. It helps ensure the circuit works well at a wide range of frequencies. Then, inductive peaking involves adding an inductor at the beginning of the circuit to boost its performance at a specific frequency. Additionally, the design favours an inductive booster at the input rather than a series booster in the feedback loop because a Series booster offers more control over the circuit's overall frequency response, and it is generally more stable and easier to implement than using inductors at the input. So, the design focuses on improving performance by adjusting the feedback loop rather than adding inductors at the input.

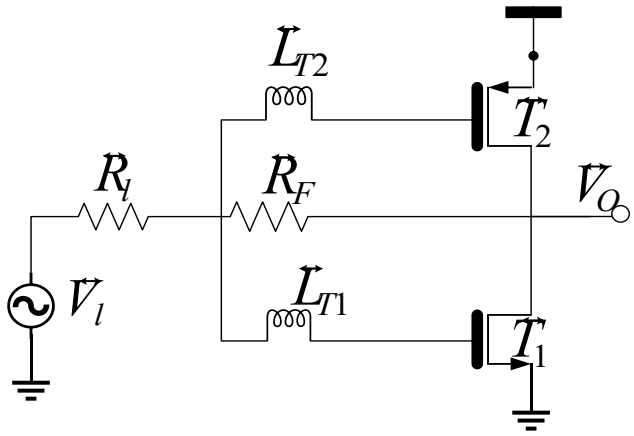


Fig. 6 Proposed shunt based resistive feedback

To achieve this, matching inductors$\vec{L}_{T1}$ in the nMOS transistor and $\vec{L}_{T2}$ the pMOS transistor are placed in series resonators, as shown in Figure 6. Using both transistors might indicate a differential or a complementary topology, where one conducts when the other is off, allowing for efficient signal processing and power consumption. This includes better noise rejection, common-mode noise cancellation, and increased linearity.

The LNA series resonators modified circuit diagram is given in Figure 7. $\vec{C}_{PAD}$ is padded capacitance with induced capacitance $\vec{C}_{as1}$ at transistor 1 and capacitance at transistor $2\vec{C}_{as2}$, drain to source capacitance at both transistor $1\vec{C}_{DS1}$ and transistor $2\vec{C}_{DS2}$ with $\vec{r}_{O1}$, $\vec{r}_{O2}$, as the output resistance. Here, inductors inside the feedback loop can help in enhancing the bandwidth of the amplifier. The circuit can compensate for the

inherent capacitances and other parasitic elements in the transistor and interconnects by introducing inductive peaking within the feedback loop, thereby extending the amplifier's frequency response. Inductors in the feedback loop can also contribute to the amplifier's stability. Properly designed feedback networks can help stabilize the amplifier against variations in load impedance, component tolerances, and environmental conditions, ensuring reliable operation across different operating conditions.

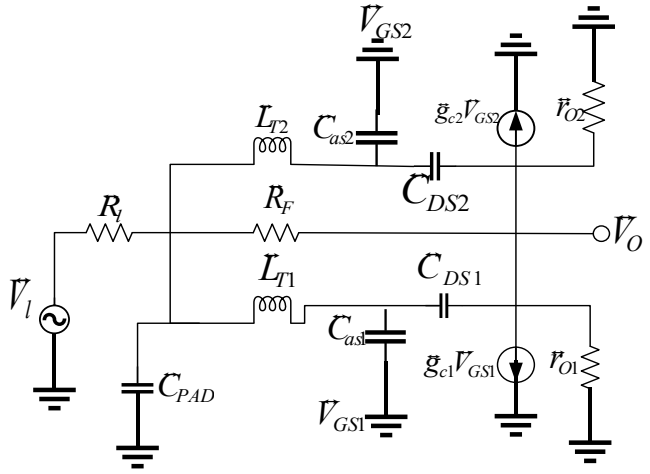


Fig. 7 Proposed modified shunt based resistive feedback

The pad capacitance in the amplifier at the input causes some distortion in signals with high data transmission speed and reduces the bandwidth. So, by introducing inductors inside the feedback loop, the MOS capacitances $\vec{C}_{as}$ $\vec{C}_{aD}$ are effectively split from "pad capacitance," which typically refers to the capacitance present at the input of the amplifier. This separation helps in reducing the impression of these capacitances' total presentation of the amplifier and facilitates bandwidth extension. MOS capacitances can limit the high-frequency performance of the amplifier by forming low-pass filter effects. The circuit can achieve a better high-frequency response and improved bandwidth by isolating them. The presence of inductors inside the feedback loop alters the impedance seen at the input of the amplifier. This change in impedance affects the feedback network's behaviour, leading to a broadening of the bandwidth of the feedback loop. This broader bandwidth is essential for maintaining stability and ensuring proper operation across a wider range of frequencies. From a pole-zero perspective, incorporating inductors inside the feedback loop shifts the circuit's main poles towards higher frequencies. This is advantageous because it helps to mitigate the effects of parasitic elements and improves the overall frequency response of the amplifier.

4.4. Parameter Extraction

Input matching ensures that the amplifier's input impedance matches the impedance of the preceding stage or the source to which it is connected. This matching is crucial for maximizing power transfer, minimizing reflections, and optimizing the amplifier's performance. The amplifier's input impedance is changed across various frequencies when inductive peaking is applied inside the feedback loop. Therefore, it becomes essential to consider the impact of inductive peaking on input matching while designing the amplifier. Deliberately adjusting specific frequencies in the circuit so that they all do not peak or dip at the same point is noted. Impedance to the design is given in Equation (6).

$$\vec{Z}_{IN} = \frac{\vec{Z}_{T1} \| \vec{Z}_{T2} \| (\vec{R}_F + \vec{r}_{O1} \| \vec{r}_{O2})}{\left(\frac{\vec{g}_{C1}(\vec{r}_{O1} \| \vec{r}_{O2})}{jw\vec{C}_{as1}\vec{Z}_{T1}} + \frac{\vec{g}_{C2}(\vec{r}_{O1} \| \vec{r}_{O2})}{jw\vec{C}_{as2}\vec{Z}_{T2}} \right)} \tag{6}$$

Where impedance in transistor $1\vec{Z}_{T1} = jw\vec{L}_{T1} + \frac{1}{jw\vec{C}_{as1}}$ and impedance in transistor $2\vec{Z}_{T2} = jw\vec{L}_{T2} + \frac{1}{jw\vec{C}_{as2}}$. This resonance circuit can selectively boost the gain of the amplifier at certain frequencies, effectively enhancing its performance in those frequency bands. The inductive element, in combination with the parasitic capacitances, forms a resonant tank circuit. At the resonant frequency, the impedance of the tank circuit is minimized, allowing maximum voltage gain. The gain produced in the circuits for high frequency is given in Equation (7).

$$\vec{A}_{oVG} = \frac{(\vec{r}_{O1} \| \vec{r}_{O2}) \left(1 - \frac{\vec{g}_{c1}\vec{R}_F}{jw\vec{C}_{as1}\vec{Z}_{T1}} - \frac{\vec{g}_{c2}\vec{R}_F}{jw\vec{C}_{as2}\vec{Z}_{T2}} \right)}{\left(\vec{R}_F + (\vec{r}_{O1} \| \vec{r}_{O2}) \right) \left(1 + \frac{\vec{R}_l}{\vec{Z}_{T1} \| \vec{Z}_{T2}} \right)} \tag{7}$$

The noise figure to the design is given as shown in Equation (8). Where the minimum possible noise factor that can be achieved, which is 1, is expressed with the first term, then the noise contributed by the feedback resistor $\vec{R}_F$ is noted in the second term. This term becomes significant when the feedback resistor value is comparable to the source resistance, which is the transistors' transconductance. Moreover, the noise from the transistor is considered in the third term. Here, the total transconductance $\vec{g}_{ct}$ is taken to increase the performance by reducing the noise figure.

$$\overleftrightarrow{NF_o} \approx 1 + \frac{\vec{R}_F}{\vec{R}_l} \left(\frac{1 + \vec{g}_{ct}\vec{R}_l}{1 - \vec{g}_{ct}\vec{R}_F} \right)^2 + \frac{\tau \vec{g}_{ct}}{\phi \vec{R}_l} \left(\frac{\vec{R}_l + \vec{R}_F}{1 - \vec{g}_{ct}\vec{R}_F} \right)^2 \tag{8}$$

A buffer acts as a protective shield between the input and output in an LNA. It ensures that the signal coming into the amplifier matches what the amplifier expects, making everything run smoothly. This buffer also keeps the input signal safe from any changes or issues in the output, maintaining its cleanliness and integrity. Additionally, the buffer helps the amplifier stay strong and steady by preventing the input signal source from overloading and ensuring consistent performance. Furthermore, if the amplifier needs to send the signal to multiple places, the buffer helps split it without causing problems. Essentially, the buffer in an LNA is like a helpful assistant that keeps everything in order,

protects the input signal, and ensures the amplifier works effectively. Finally, it gives good linearity and reduces noise by reducing power consumption. However, the gain of the amplifier is relatively low. The peaking inductors used in the design aid in broadening the amplifier's bandwidth and contribute to a reduction in overall gain. So, to overcome this issue, PSO has been adopted for the proposed design.

4.5. Optimization

PSO is commonly used in optimization problems where the search space is continuous and differentiable. It is particularly well-suited for problems with many local optima, as the swarm's collective behaviour helps to explore the search space effectively [23]. PSO is applied during the design optimization phase of the PSbSF-TCR LNA, targeting the selection and tuning of component values such as the shunt feedback resistance, transformer coupling coefficient, resonator inductance and capacitance, and biasing parameters. These parameters significantly influence the LNA's gain, bandwidth, noise figure, and impedance matching. PSO searches for the optimal configuration that meets multiple design objectives by encoding these variables into particles. Constraints are imposed to maintain power consumption within practical limits and to satisfy stability conditions over the mmWave frequency range.

- PSO starts by initializing a particle population. Every Particle is a possible answer to the optimization issue.
- Based on its own experiences and those of its neighbours, each Particle modifies its position and velocity. This is adjusted based on its current speed, how far it is from its best-known solution, and how far it is from the best solution found by any nearby particle. The position update$T_{pq}(i+1)$ is then performed in Equation (10) based on the new velocity$S_{pq}(i+1)$ shown in Equation (9).

$$S_{pq}(i+1) = gS_{pq}(i) + d_1a_1\left(B_{pq}(i) - T_{pq}(i)\right) + d_2a_2\left(G_{pq}(i) - T_{pq}(i)\right) \quad (9)$$

$$T_{pq}(i+1) = T_{pq}(i) + S_{pq}(i+1) \quad (10)$$

Where, Dynamic weight coefficient is given as$g$, $d_1 and d_2$ uncertain variable with a_1 *and* a_2 are the Learning acceleration terms, Global best solution as $G_{pq}(i)$and best-obtained position as$B_{pq}(i)$.

- Each Particle updates its own best spot if it finds something better, and if any particle finds a better solution than the current best among all particles, that becomes the new best for everyone [26].
- The algorithm continues iterating through velocity and position updates until a termination condition is met.

The PSO algorithm runs iteratively, updating particle positions based on the best-found solution in each iteration, guiding the search toward globally optimal values. Each iteration's output is verified using circuit simulation tools, ensuring the design meets practical mmWave specifications.

This optimization improves the overall gain with low power consumption and noise figures. Below is the algorithm for the proposed work.

Algorithm for proposed PSbSF-TCR topology

Start
{
Design Parameter module ()
{
Int $(\vec{g}_c/\vec{g}_{rs}), \left(\vec{f}T_u\right), \vec{I}_R, \vec{g}_c, \left(\overleftrightarrow{NF}\right)$;
// considering biasing metrics

$$B_m = \frac{\left[\left(\frac{\vec{g}_c}{\vec{I}_R}\right)\bullet(\vec{g}_c/\vec{g}_{rs})\bullet\left(\vec{f}T_u\right)\right]}{\min\left(\overleftrightarrow{NF}\right)};$$

//using Equation (1)
//to meet the objectives
}
Design LNA module ()
{
Int $\vec{R}_o, \vec{R}_F, \vec{g}_c, \tau, \phi, \vec{R}_l$;
// considering input impedance for reducing current

$$\vec{I}_{in} = \frac{\vec{R}_O + \vec{R}_F}{1 + \vec{g}_c\vec{R}_O}$$

//using Equation (2)
// Average gain to the design

$$\vec{A}_{Vg} = \frac{\vec{R}_O\left(1 - \vec{g}_c\vec{R}_F\right)}{\left(\vec{R}_O + \vec{R}_F\right)}$$

//using Equation (3)
//Noise figure to the design

$$\overleftrightarrow{NF} \geq 1 + \frac{4\tau\vec{g}_c}{\phi\vec{R}_l}\left[\frac{\left(\vec{R}_O + \vec{R}_F\right)\left(\vec{R}_l + \vec{R}_F\right)}{\left(1 - \vec{g}_c\vec{R}_F\right)\left(\vec{R}_O\left(1 + \vec{g}_c\vec{R}_l\right) + \left(\vec{R}_l + \vec{R}_F\right)\right)}\right]^2$$

//using Equation (4)
// design is used to reduce power
}
Proposed PSbSF-TCR module ()
{
Int $\vec{R}_o, \vec{R}_F, \vec{g}_c, \tau, \phi, \vec{R}_l, j, w, \vec{C}_{as}$;
// transconductance is taken

$$\vec{g}_{c,eff} = \frac{\vec{g}_c}{\phi\left(1 + \frac{\vec{R}_l}{\vec{R}_F} + \frac{\vec{R}_l}{\vec{R}_F^2}\vec{R}_a\left(\vec{g}_c\vec{R}_F - \phi\right) + \frac{jw\vec{C}_{as}\vec{R}_l}{\phi}\right)}$$

//using Equation (5)
//taken for peaking circuit
}
Parameter Extraction module ()
{

Int $\vec{Z}_{T1}, \vec{Z}_{T2}, \vec{r}_{O1}, \vec{r}_{O1}, \vec{R}_o, \vec{R}_F, \vec{g}_c, \tau, \phi, \vec{R}_l, j, w, \vec{C}_{as1}, \vec{C}_{as2}$
//Proposed input impedance is taken

$$\vec{Z}_{IN} = \frac{\vec{Z}_{T1} \| \vec{Z}_{T2} \| (\vec{R}_F + \vec{r}_{O1} \| \vec{r}_{O2})}{\left(\frac{\vec{g}_{C1}(\vec{r}_{O1} \| \vec{r}_{O2})}{jw\vec{C}_{as1}\vec{Z}_{T1}} + \frac{\vec{g}_{C2}(\vec{r}_{O1} \| \vec{r}_{O2})}{jw\vec{C}_{as2}\vec{Z}_{T2}} \right)} \quad //$$

using Equation (6)
//average gain is taken

$$\vec{A}_{oVG} = \frac{(\vec{r}_{O1} \| \vec{r}_{O2}) \left(1 - \frac{\vec{g}_{c1}\vec{R}_F}{jw\vec{C}_{as1}\vec{Z}_{T1}} - \frac{\vec{g}_{c2}\vec{R}_F}{jw\vec{C}_{as2}\vec{Z}_{T2}} \right)}{(\vec{R}_F + (\vec{r}_{O1} \| \vec{r}_{O2})) \left(1 + \frac{\vec{R}_l}{\vec{Z}_{T1} \| \vec{Z}_{T2}} \right)}$$

//using Equation (7)
//noise figure is taken

$$\overleftrightarrow{NF_o} \approx 1 + \frac{\vec{R}_F}{\vec{R}_l} \left(\frac{1 + \vec{g}_{ct}\vec{R}_l}{1 - \vec{g}_{ct}\vec{R}_F} \right)^2 + \frac{\tau \vec{g}_{ct}}{\phi \vec{R}_l} \left(\frac{\vec{R}_l + \vec{R}_F}{1 - \vec{g}_{ct}\vec{R}_F} \right)^2$$

//using Equation (8)
//all parameters are extracted
}
Optimization module ()
{
Int $B_{pq}(i), g, a_1 and a_2, G_{pq}(i), d_1 and d_2, T_{pq}(i+1), S_{pq}(i+1)$;
//velocity is updated

$$S_{pq}(i+1) = gS_{pq}(i) + d_1 a_1 \left(B_{pq}(i) - T_{pq}(i) \right) + d_2 a_2 \left(G_{pq}(i) - T_{pq}(i) \right);$$

//using Equation (9)
// position is updated

$$T_{pq}(i+1) = T_{pq}(i) + S_{pq}(i+1);$$

//using Equation (10)
//continued till values are optimized
}
}
Stop

Figure 8 shows the workflow of the adopted PSbSF-TCR design. First, bandwidth, frequency, gain, and power consumption are considered in the design. These values are given in Table 2.

Table 2. Input parameters

Frequency Band	28 GHz - 29 GHz
Bandwidth	1 GHz
Gain	20 dB
Noise Figure	1.5 dB
Power Consumption	15.98 mW

Then, shunt feedback is developed to reduce the power consumption in the design process. The proposed PSbSF-TCR is modelled specially to reduce power consumption by improving bandwidth.

This is efficiently done by simultaneously reducing noise figures. A protection with a buffer is given to the circuit so as not to disturb the input and output parameters. Then, parameters are extracted as given in Table 3.

Table 3. Extracted parameters

Gain	28 dB
Noise figure	5.79 dB
Power consumption	12.69 mW
Bandwidth	49 GHz

However, it cannot be improved, and overall improvement is insufficient. So, a new PSO technique is used to improve performance. This uses the knowledge of swarms. They are brilliant at managing the positions between them to reach the target. Similar work is utilized here to update the position of each parameter step by step, and overall, it improves the design's performance. The values obtained after optimization are given as Gain: 45.00 dB, Noise Figure: 1.37 dB, Bandwidth: 69.10 GHz, Latency: 0.37 seconds, Voltage: 0.47 volts, Power Consumption: 6.78 mW, Frequency Response: 400.00 GHz.

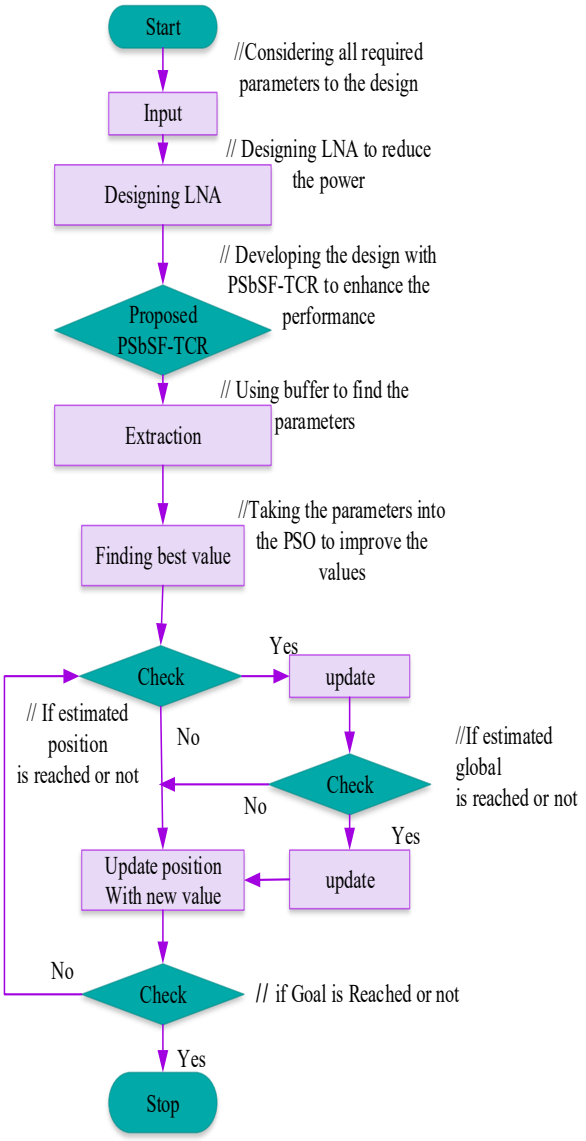


Fig. 8 Flowchart to the developed design PSbSF-TCR

5. Result of the Proposed PSbSF-TCR

The performance of the proposed PSbSF-TCR is discussed in this section. This shows how well the proposed PSbSF-TCR reduced power consumption with low noise and improved overall design gain. This circuit is fabricated using a 45-nanometer process.

The proposed model is designed in MATLAB, and simulation performances are performed using that platform. The performance matrices are Power consumption, Noise figure, Bandwidth, Latency, Gain, Voltage, and Frequency.

5.1. Power Consumption

The energy the design utilizes to receive or transmit the signal is calculated through power consumption. It discusses how well the design is modified and improved in its usage. For the best design, power consumption should be very low. PSbSF-TCR power consumption is given in Figure 9.

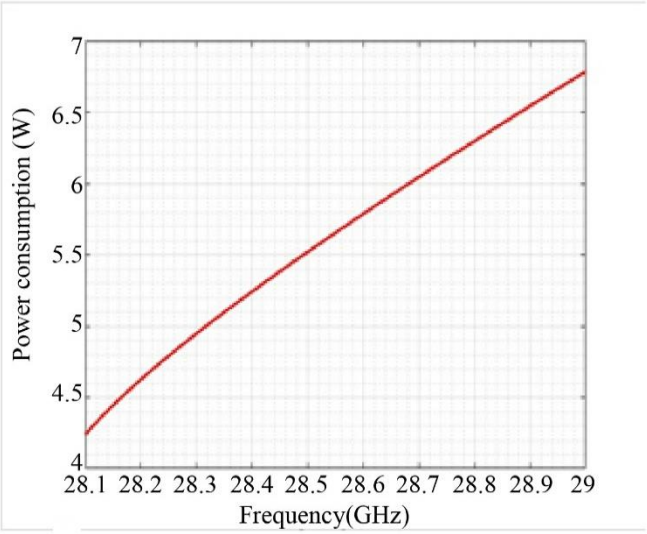


Fig. 9 Power consumption for developed PSbSF-TCR

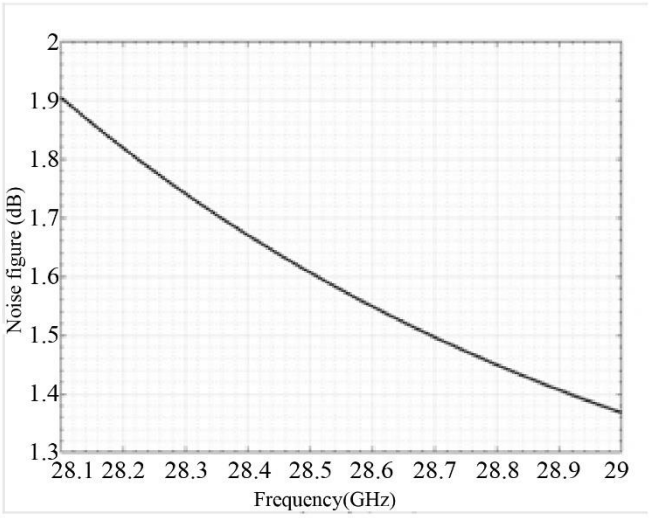


Fig. 10 Noise figure to the developed PSbSF-TCR

5.2. Noise Figure

The noise figure measures how much noise a device adds to the signal in processes. Lower noise figures indicate better performance because they imply that the device adds less noise, preserving more of the original signal's quality.

$$\overleftrightarrow{NF} = 10\,log\left(\frac{\overline{S_{NR}}_{in}}{\overline{S_{NR}}_{out}}\right) \tag{11}$$

Equation (11) gives a noise figure $\overleftrightarrow{NF}$ using the signal-to-noise ratio at input $\overline{S_{NR}}_{in}$ to the signal-to-noise ratio at output $\overline{S_{NR}}_{out}$. The PSbSF-TCR noise figure is given in Figure 10.

5.3. Bandwidth

It can denote the capacity of a communication channel to carry data, the range of frequencies within a signal, or the operational capability of an electronic circuit. Higher bandwidth typically implies greater capacity or capability, such as faster data transfer rates in communication systems or the ability to process a broader range of frequencies in signal-processing applications. PSbSF-TCR bandwidth is given in Figure 11.

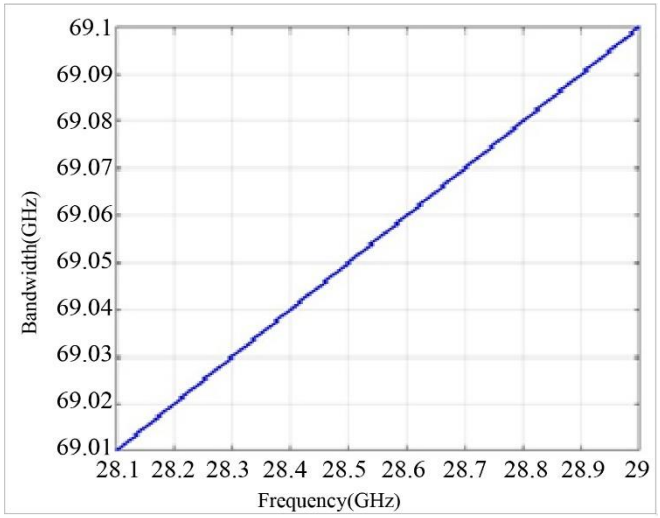


Fig. 11 Bandwidth to the developed PSbSF-TCR

5.4. Latency

The time the design takes to transmit or receive the messages is estimated through latency. High latency can lead to delays in data transmission, impacting the responsiveness of applications, especially those requiring real-time interaction, such as online gaming, video conferencing, and financial trading.

$$\overleftrightarrow{L} = \frac{b_P}{d_R} \tag{12}$$

Latency $\overleftrightarrow{L}$ to the proposed design is given in Equation (12) by using bit packet b_P and data rate d_R. PSbSF-TCR latency is given in Figure 12.

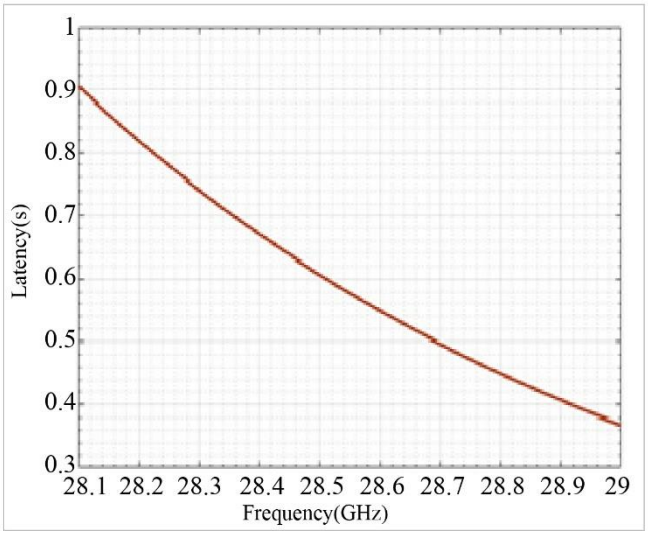


Fig. 12 Latency to the developed PSbSF-TCR

5.5. Gain

Gain $\vec{G}_T$ in an LNA refers to the amplification factor provided by the amplifier while introducing minimal additional noise to the signal. The gain of an LNA is typically expressed in decibels (dB) and represents the ratio of the output signal powerW_{out} to the input signal powerW_{in}. A higher gain indicates that the LNA amplifies the input signal more effectively. PSbSF-TCR gain is shown in Figure 13.

$$\vec{G}_T = 10\, log_{10}\left(\frac{W_{out}}{W_{in}}\right) \tag{13}$$

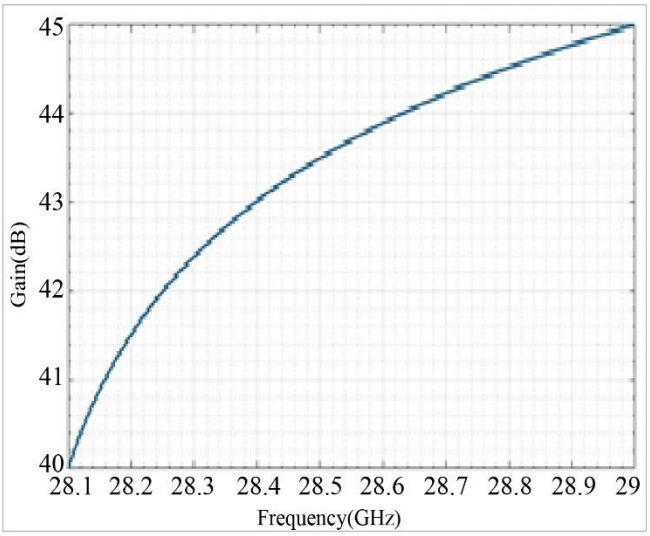


Fig. 13 Gain to the developed PSbSF-TCR

5.6. Voltage

The force given to the circuit to run the task is estimated through voltage. This supply voltage is important to determine the amount of energy available to perform electrical work or drive various components. Voltage to the developed PSbSF-TCR is given in Figure 14.

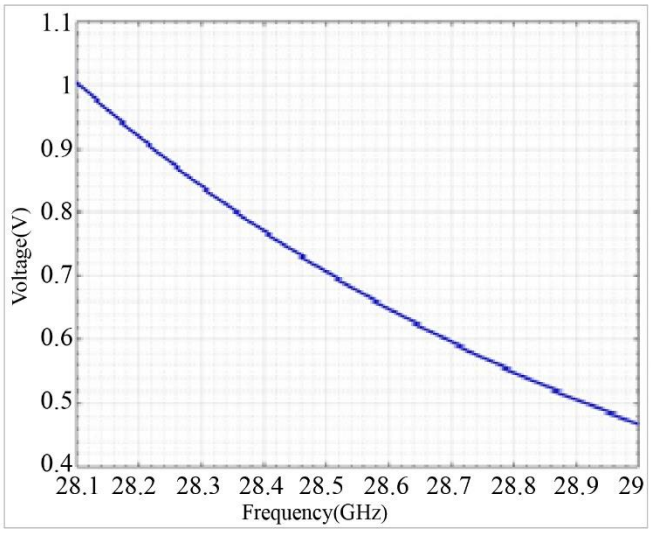


Fig. 14 Voltage to the developed PSbSF-TCR

5.7. Frequency

The LNA must be designed to amplify signals within a specific frequency range relevant to the application. The system's bandwidth requirements often determine this frequency range. Figure 15 shows the frequency of the developed PSbSF-TCR.

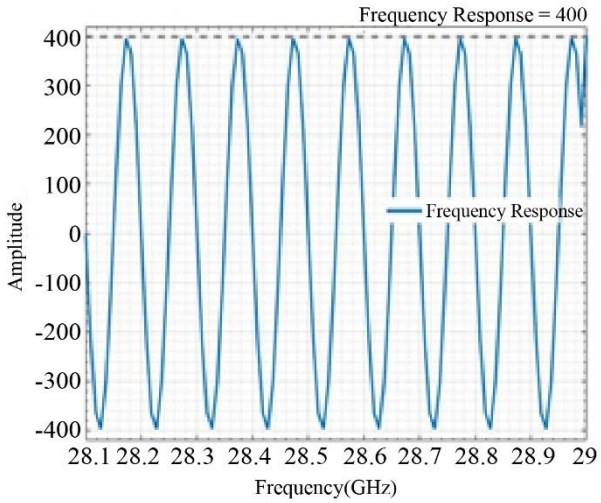


Fig. 15 Frequency to the developed PSbSF-TCR

6. Comparative Estimation

The proposed method is compared with other existing methods like Nano Vertical III-V Wires-VbNW, Fully Depleted Silicon On Insulator-FDSOI, Silicon Germanium technology to fabricate Heterojunction Bipolar Transistors - SiGe HBT, Indium Gallium Arsenide High Electron Mobility Transistor- InGaAs HEMT [27] for gain, Frequency, bandwidth and noise Figure and wake-up receiver fully integrated RF-SOI CMOS- WRFI-SOI CMOS, CMFB CMOS- Common mode feedback CMOS, PLL- CMOS- Phase lock loop CMOS [28] for latency and voltage. Triple

Cross-Coupling technique (TCC), Impedance Matching Feed-Forward technique (IMFF), Inductor less Wideband low-noise Amplifier (IWA), and Derivative Superposition Technique (DST) for S11, S22, IIP3, area and FOM [25]. Comparative values of frequency, bandwidth, gain, and noise figures are given in Table 4.

Table 4. Comparative table for the developed design PSbSF-TCR

Metrics	Proposed PSbSF-TCR	VbNW [27]	FDSOI p [27]	SiGe HBT [27]	InGaAs HEMT [27]
Technology	45 nm CMOS	20 nm MOSFET	22 nm CMOS	90 nm CMOS	50 nm CMOS
Frequency [GHz]	400	360	240	300	380
bandwidth [GHz]	69.10	30	40	28	67
Gain [dB]	45	23	16	30	30.8
Power consumption[mW]	6.78	11.4	44	45	57.6
Noise figure [dB]	1.37	2.5	8.5	6.2	3

6.1. Comparative Estimation of Power Consumption

A comparative estimation of the developed PSbSF-TCR design with other existing techniques is shown in Figure 16. It is seen that the HEMT method had taken 57.6mW of power to run the design. By reducing this level, HBT used 45 mW of power to run the design. Then, FDSOI used 44 mW of power and reduced the power usage. Moreover, VbNW used 11.4 mW of power, whereas the proposed PSbSF-TCR used 6.78 mW of power and overcame other techniques, making the design the most suitable.

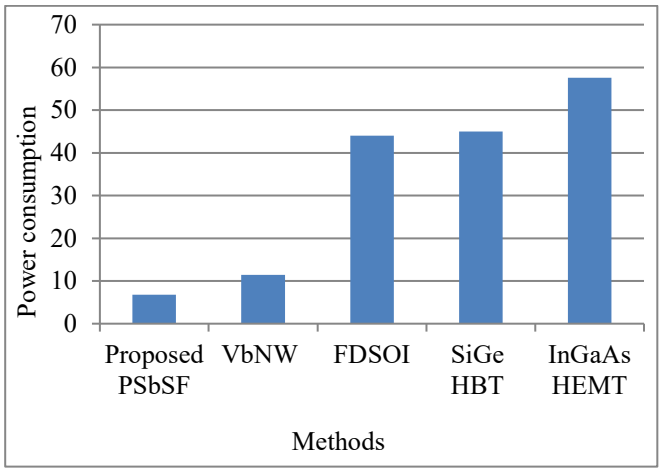


Fig. 16 Comparative on power consumption for developed PSbSF-TCR

6.2. Comparative Estimation of Noise Figure

A comparative estimation of the noise figure is shown in Figure 17. The PSbSF-TCR technology exhibits an exceptionally low noise figure of 1.37 dB, indicating its potential for applications demanding minimal signal degradation and high sensitivity. In contrast, the VbNW and InGaAs HEMT technologies display higher noise figures of 2.5 dB and 3 dB, respectively, suggesting a diminished ability to maintain signal purity and fidelity. The FDSOI technology shows a relatively higher noise figure of 8.5 dB, which may limit its suitability for applications requiring stringent noise performance. Meanwhile, the SiGe HBT technology falls in the middle ground with a noise figure of 6.2 dB, balancing amplification and noise characteristics.

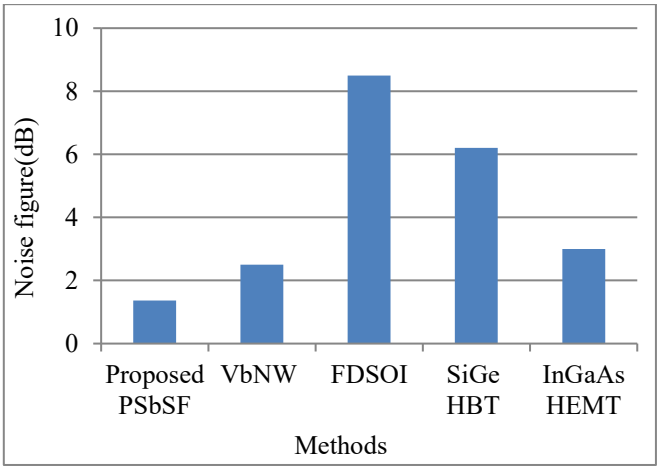


Fig. 17 Comparative on noise figure for developed PSbSF-TCR

6.3 Comparative Estimation of Bandwidth

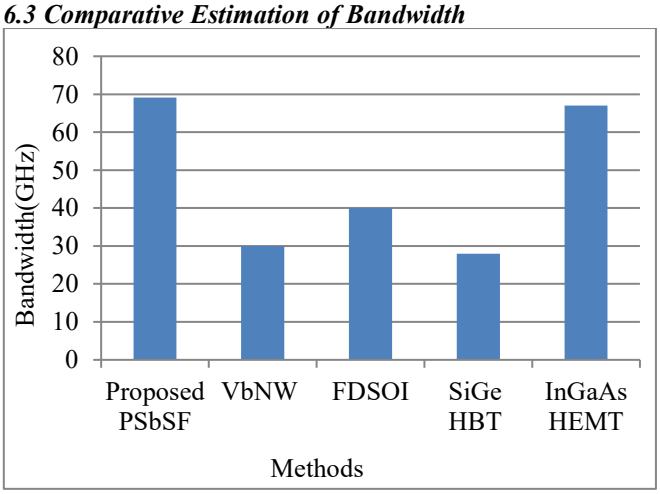


Fig. 18 Comparative of bandwidth for developed PSbSF-TCR

Comparing the bandwidth performance across the proposed PSbSF-TCR, VbNW, FDSOI, SiGe HBT, and InGaAs HEMT technologies reveals significant variations, as given in Figure 18. The PSbSF-TCR technology exhibits the widest bandwidth of 69.10 GHz, indicating its capability to handle high-frequency signals effectively. In contrast, the VbNW technology offers a comparatively lower bandwidth of

30 GHz, suggesting limitations in accommodating broader frequency ranges. The FDSOI and SiGe HBT technologies fall in between, with bandwidths of 40 GHz and 28 GHz, respectively. The InGaAs HEMT technology showcases a substantial bandwidth of 67 GHz, trailing closely behind the PSbSF-TCR technology.

6.4. Comparative Estimation of Latency

Comparing the latency as given in Table 5, the specifications of the proposed technologies shed light on their operational efficiency and responsiveness, crucial factors for various applications. Among the methods in the table, PSbSF-TCR boasts the lowest latency, with a swift response time of 0.37 seconds. This rapid processing capability positions PSbSF-TCR as an attractive choice for applications where real-time data processing or low-latency communication is paramount, such as in telecommunications or sensor networks. Following PSbSF-TCR, PLL demonstrates respectable latency performance, with a response time of 0.54 seconds. While slightly higher than PSbSF-TCR, PLL still offers competitive latency that is suitable for many applications. Conversely, WRFI-SOI exhibits a latency of 0.486 seconds, placing it between PSbSF-TCR and PLL regarding responsiveness, as given in Figure 19. CMFB, with a latency of 1.0 seconds, presents the highest delay among the technologies considered.

Table 5. Comparative values for voltage and latency

Metrics	Proposed PSbSF-TCR	WRFI-SOI	CMFB	PLL
Technology	45 nm CMOS	45 nm CMOS	65 nm CMOS	65 nm CMOS
Voltage (v)	0.47	1.0	0.4	1.0
Latency (s)	0.37	0.486	1.0	0.54

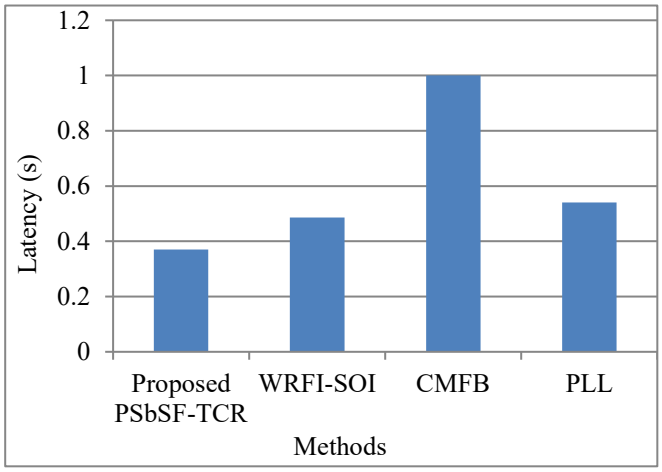


Fig. 19 Comparative on latency for developed PSbSF-TCR

6.5. Comparative Estimation of Gain

The comparison of gain performance among different technologies reveals intriguing insights into their respective suitability for various applications. Among all the previous techniques, the proposed PSbSF-TCR technology stands out with its impressive gain of 45 dB, marking it as a promising candidate for high-performance applications where amplification is crucial, as given in Figure 20. The SiGe HBT and InGaAs HEMT technologies are closely behind, offering substantial gains of 30 dB and 30.8 dB, respectively, making them well-suited for various applications requiring reliable amplification. However, VbNW and FDSOI technologies lag in gain, with values of 23 dB and 16 dB, respectively.

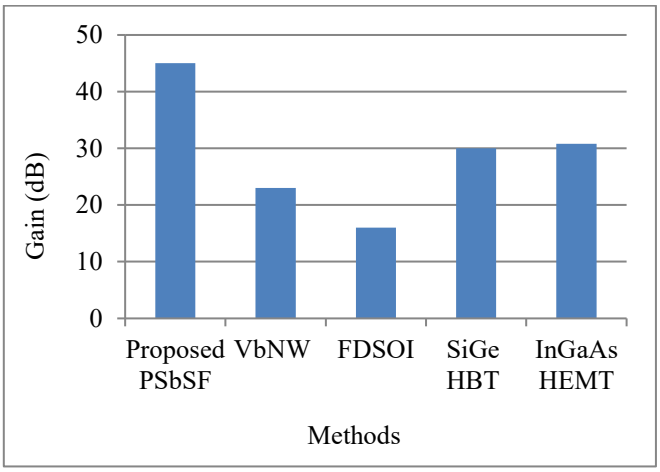


Fig. 20 Comparative on gain for developed PSbSF-TCR

6.6. Comparative Estimation of Voltage

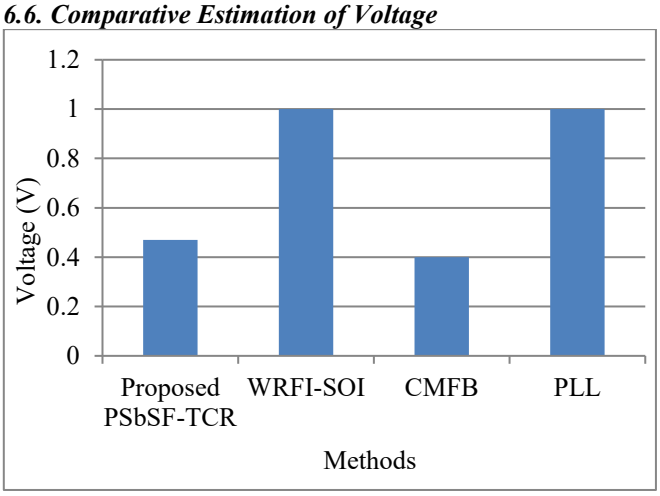


Fig. 21 Comparative on voltage for developed PSbSF-TCR

When comparing the voltage specifications of the proposed technologies, namely PSbSF-TCR, WRFI-SOI, CMFB, and PLL, distinct differences emerge that significantly affect their performance and power efficiency. Among these technologies, CMFB stands out with the lowest voltage requirement, operating at just 0.4 volts.

This low voltage demand positions CMFB as a highly power-efficient option, particularly suitable for applications prioritizing energy conservation. In contrast, WRFI-SOI and PLL operate at a higher voltage of 1.0 volts, indicating

potentially higher power consumption than CMFB. PSbSF-TCR falls between these extremes, with a voltage specification of 0.47 volts, presenting a moderate power efficiency profile as given in Figure 21.

6.7. Comparative Estimation of Frequency

Regarding frequency performance, the proposed PSbSF-TCR technology stands out with an impressive capability of 400 GHz, making it suitable for ultra-high-speed applications, as shown in Figure 22. Following closely is the InGaAs HEMT technology with a frequency of 380 GHz, offering robust performance in high-frequency domains. VbNW and SiGe HBT technologies exhibit frequencies of 360 GHz and 300 GHz, respectively, demonstrating competitive performance in terms of frequency. Conversely, FDSOI technology lags with a frequency of 240 GHz, indicating its limitations in ultra-high-frequency applications. Therefore, for applications where frequency is a critical factor, PSbSF-TCR technology presents a promising option, offering superior performance in high-frequency operations.

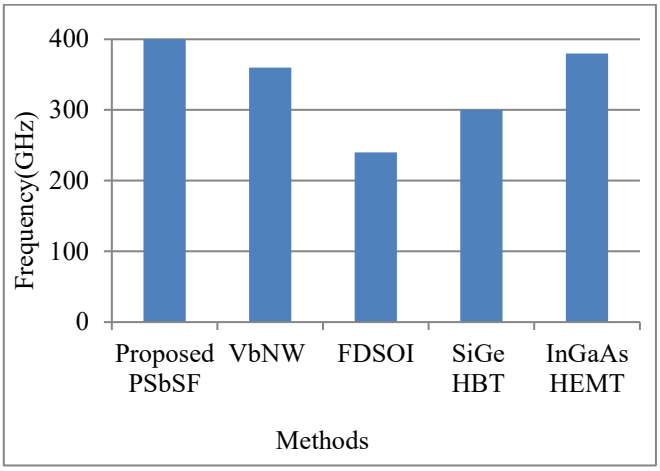


Fig. 22 Comparative of frequency for developed PSbSF-TCR

Table 6. Comparative values for S11, S22, IIP3, area and FOM

Method	Process	S11 (dB)	S22 (dB)	IIP3 (dBm)	Area (mm²)	FOM
TCC	180nm CMOS	<-10	<-13	14–21	0.27	63.34
DST	90	<-3	<-7	18.3	0.7	10.7
IWA	180µm CMOS	<-7.8	<-2	0.25	0.055	9.5
IMFF	65	<-10	<-8	-5	0.16	8.16
Proposed	45nm SOI MOSFET	<-15	<-12	22	0.045	120.4

6.8. Comparative on S11

S11 represents the input return loss, with more negative values indicating better input matching. Among all the designs, the proposed 45nm SOI MOSFET achieves the best input matching with an S11 of less than -15 dB. This is a significant improvement, especially compared to DST, which exhibits the poorest input return loss at less than -3 dB. TCC and IMFF provide reasonably good values at less than -10 dB, while IWA is slightly weaker at less than -7.8 dB. Overall, the proposed design performs better in minimizing signal reflections at the input. Table 6 gives the comparative values for S11, S22, IIP3, Area and FOM and comparative graphs are shown in Figure 23.

6.9. Comparative on S22

S22 measures output return loss, where lower values again reflect better output matching. TCC leads slightly in this category with an S22 of less than -13 dB, closely followed by the proposed design at less than -12 dB. IMFF and DST offer moderate values of less than -8 dB and -7 dB, respectively. However, IWA performs poorly here, with an S22 of less than -2 dB, indicating significant output signal reflection. The proposed design's near-best value confirms its strong output interface characteristics.

6.10. Comparative on IIP3 (Third-Order Input Intercept Point)

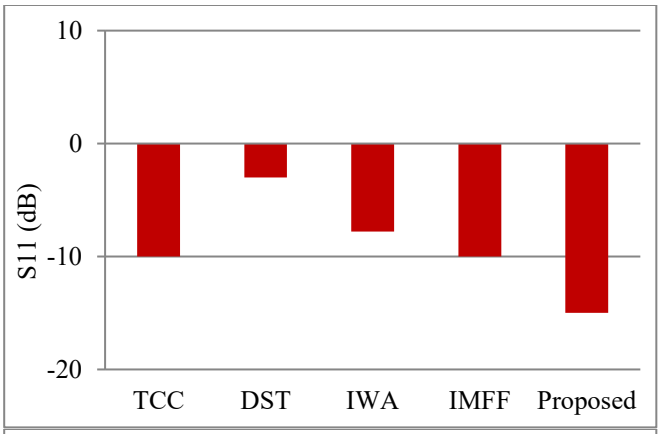
IIP3 is a crucial parameter that reflects a system's linearity, with higher values indicating better performance. The proposed 45nm SOI MOSFET design exhibits the highest linearity with an IIP3 of 22 dBm. DST follows with 18.3 dBm, while TCC ranges between 14 and 21 dBm. IWA falls short with a very low IIP3 of 0.25 dBm, and IMFF performs worst with a negative IIP3 of -5 dBm. This establishes the proposed design's excellence in handling high-input signals with minimal distortion.

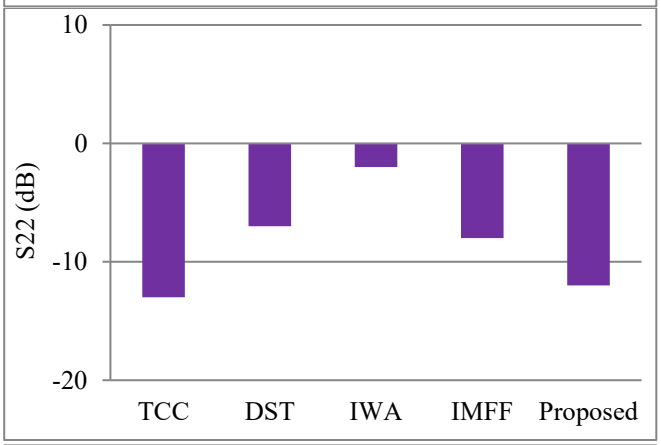
6.11. Comparative on Area

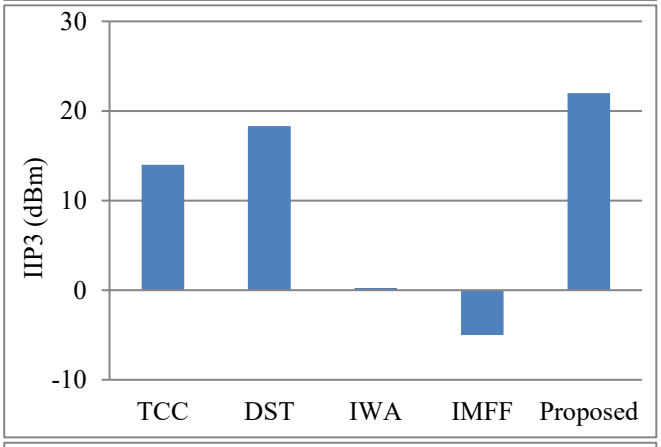
In terms of physical area, a smaller footprint is generally desirable for integration and cost-efficiency. The proposed design also excels in this metric, requiring only 0.045 mm², making it the most compact solution among the compared references. IWA also achieves a small area of 0.055 mm². IMFF and TCC are moderate at 0.16 mm² and 0.27 mm², respectively, while DST has the largest area at 0.7 mm². The proposed design's minimal area requirement makes it highly suitable for space-constrained applications.

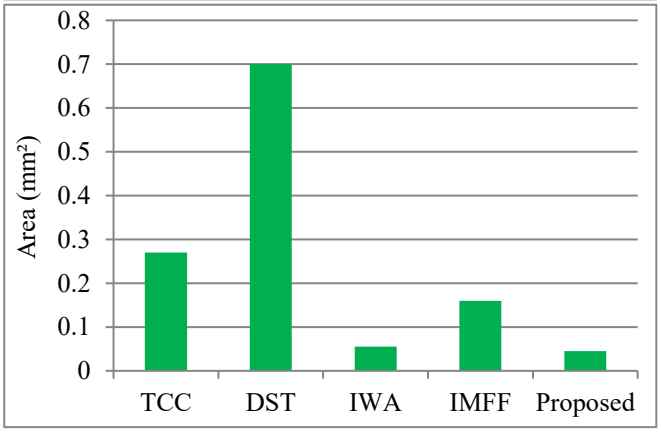
6.12. Comparative on FOM (Figure of Merit)

The Figure of Merit combines various performance aspects into a single value to indicate design efficiency. Here, the proposed design achieves a remarkable FOM of 120.4, surpassing all other designs. TCC comes next with a FOM of 63.34, nearly half that of the proposed design. DST, IWA, and IMFF lag significantly with FOMs of 10.7, 9.5, and 8.16, respectively. This outstanding FOM solidifies the proposed design's position as the most effective and well-balanced solution among its peers.









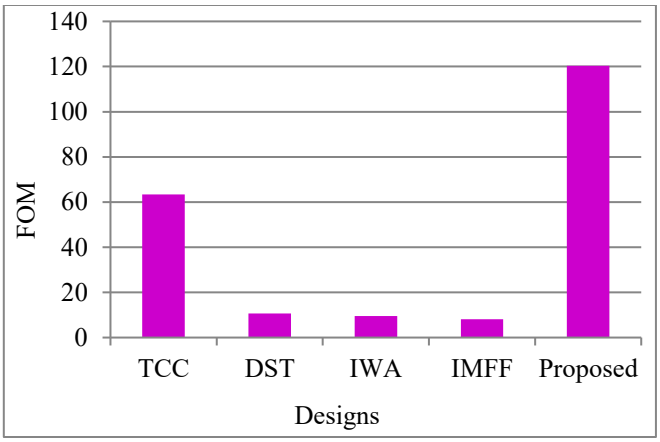


Fig. 23 Comparison on S11, S22, IIP3, area and FOM

7. Discussion

The performance of the proposed architecture significantly outperforms existing designs in terms of frequency coverage, NF, and gain, as highlighted by Tables 3 and 4. VbNW MOSFETs operate for mm-wave, but their work was constrained by integration challenges at higher frequencies and limited gain stability. In contrast, the proposed method leverages a compact, high-gain D-band LNA architecture, which ensures broader bandwidth and better integration for system-on-Chip (SoC) applications. A band-configurable WRFI-SOI operating at 5.5–7.5 GHz uses 45-nm RF-SOI CMOS. While efficient in power handling, its low-frequency limitation and narrower tuning range make it unsuitable for D-band applications. The proposed method, operating in the 122–150 GHz range with stable performance metrics, addresses these limitations by achieving higher frequency operation with enhanced linearity and lower power consumption.

InGaAs HEMT using 100 and 50 nm with 50% bandwidth and a 3.0 dB noise figure. While this is commendable, the proposed design achieves competitive bandwidth while reducing NF further, as evident in Table 4 shows a lower average NF and improved signal gain. This is attributed to our circuit design's optimized multi-stage amplifier layout and impedance matching strategies. A broadband transmitter/receiver using 22nm FDSOI CMOS, though compact and broadband, the system's NF and linearity were less favorable under high-frequency noise. The proposed method integrates advanced biasing and matching techniques that significantly reduce phase noise and improve gain uniformity, addressing those shortcomings.

A SiGe HBT BiCMOS LNA operating in the 122–150 GHz band achieves a 30 dB gain with a 6.2 dB noise figure, demonstrating superior performance. However, the proposed design surpasses this by delivering both a higher gain and a substantially lower NF, as demonstrated in Table 3. Moreover, Table 4 highlights our design's superior energy efficiency and linear performance across varied temperature and load

conditions, a critical advantage in real-world D-band transceiver applications. The IMFF technique is used in a packaged noise-canceling wideband LNA that achieves high gain and improved linearity across a broad frequency range.

However, external packaging introduces parasitic effects that degrade performance at higher frequencies, limiting its applicability in compact mmWave systems. TCC is applied in an ultra-low power CMOS LNA, delivers excellent energy efficiency, and is well-suited for WPAN applications. Nonetheless, its performance is restricted to lower frequency bands and lacks the gain and bandwidth necessary for mmWave or 5G systems. IWA simplifies the circuit layout by eliminating inductors and applying a noise cancellation strategy to enhance integration.

However, the absence of inductors compromises gain enhancement and impedance matching at high frequencies. DST improves linearity by minimizing distortion through nonlinear cancellation but comes at the cost of increased circuit complexity and higher power consumption, which is unsuitable for compact or low-power designs.

In contrast, the proposed PSbSF-TCR architecture effectively addresses these limitations by integrating shunt feedback, transformer-coupled resonators, and PSO-based optimization. This approach achieves a well-balanced performance, delivering high gain, low noise figure, wide bandwidth, and energy efficiency, making it ideal for next-generation 5G mmWave applications. Overall, the proposed approach shows a holistic enhancement in key performance indicators, including gain, noise figure, power consumption, and operating bandwidth. These improvements are realized through advanced material integration, circuit co-design, and layout optimization, validating its potential for high-frequency communication systems beyond the capabilities of previously reported methods.

8. Conclusion

The innovative approach of LNA design with the proposed method PSbSF-TCR marks a significant leap forward in amplifier technology, especially tailored for the demands of 5G networks. By leveraging advanced optimization techniques like PSO and integrating sophisticated features like Shunt Feedback and transformer-coupled resonators, it created an amplifier that outperforms traditional ones in reducing noise, amplifying signals, and handling diverse frequencies. This breakthrough holds immense promise for enhancing the performance and reliability of 5G networks, paving the way for a faster, more robust, and seamless communication experience for users worldwide.

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